

Advance Information
MCA3 ETL SERIES MACROCELL ARRAYS

This specification establishes design and performance requirements for the MCA3 ETL Series Macrocell Arrays with mixed ECL, PECL, and TTL compatible interfaces. Motorola's MOSAIC III™ process provides the MCA3 ETL Series with the logic power of 858 to 6915 equivalent 150 ps (typical) gates on one integrated circuit chip. Any signal pin can be programmed for input, output, or bidirectional signals in ECL, TTL, or PECL (pseudo-ECL) logic families. Advanced process technology, combined with innovative high-speed logic design, and an extensive macrocell library incorporating a versatile I/O structure give the arrays the performance and flexibility required to meet today's high-performance system needs.

**MCA750ETL
MCA3200ETL
MCA6200ETL**

**TTL-ECL-PECL
COMPATIBLE
MCA3 ETL SERIES
MACROCELL ARRAYS**

- Logic Function Fully Specified by User
- Metal Mask Programmable (Three Unique Masks)
- 2.5 GHz Toggle Rate on Selected D Flip-Flop Macros
- Internal ECL Gate Delays – 0.15ns Typical
- Input ECL Cell Delays – 0.15ns Typical
- Output ECL Cell Delays – 0.3ns Typical
- TTL Input/Translation Cell Delay – 0.55ns Typical
- TTL Output/Translation Cell Delay – 2.0ns Typical
- ECL 100K, 100E, PECL, and TTL Logic Interfaces
- ECL, TTL, ETL, and PETL System Combinations
- Programmable Speed/Power Levels
- Three-Level Series Gated Macros
- MCA2 and MCA3 ECL Series Library Compatibility

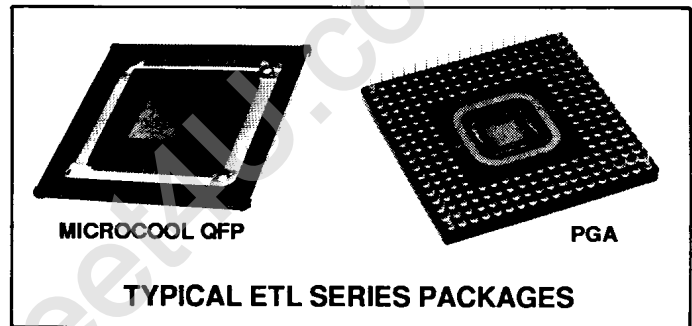


FIGURE 1 – MCA3 ETL ARRAY BASIC BLOCK DIAGRAM

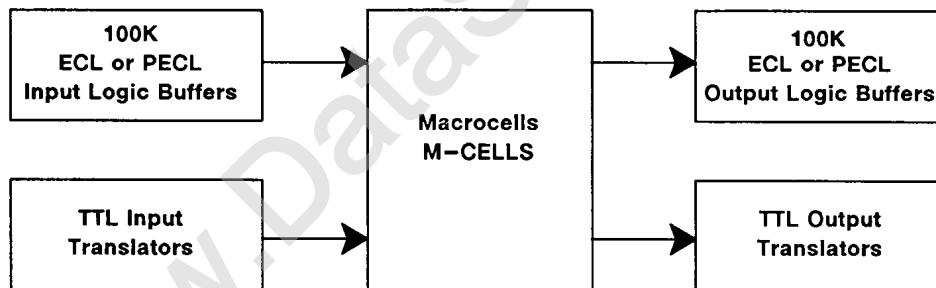


TABLE 1 – MCA3 ETL SERIES ARRAY FEATURES

| Array | # of Equivalent Gates | # of Minimum Addressable Units (MAUs) | # Of Universal I/O Cells | Die Size (mils) | Packages |
|------------|-----------------------|---------------------------------------|--------------------------|-----------------|------------------|
| MCA750ETL | 858 | 96 | 42 | 139 x 168 | 64 QFP |
| MCA3200ETL | 3570 | 440 | 120 | 268 x 268 | 169 PGA/160 QFP |
| MCA6200ETL | 6915 | 900 | 168 | 352 x 352 | 224 PGA/328 TAB* |

*Contact factory for 328 TAB package information and availability.

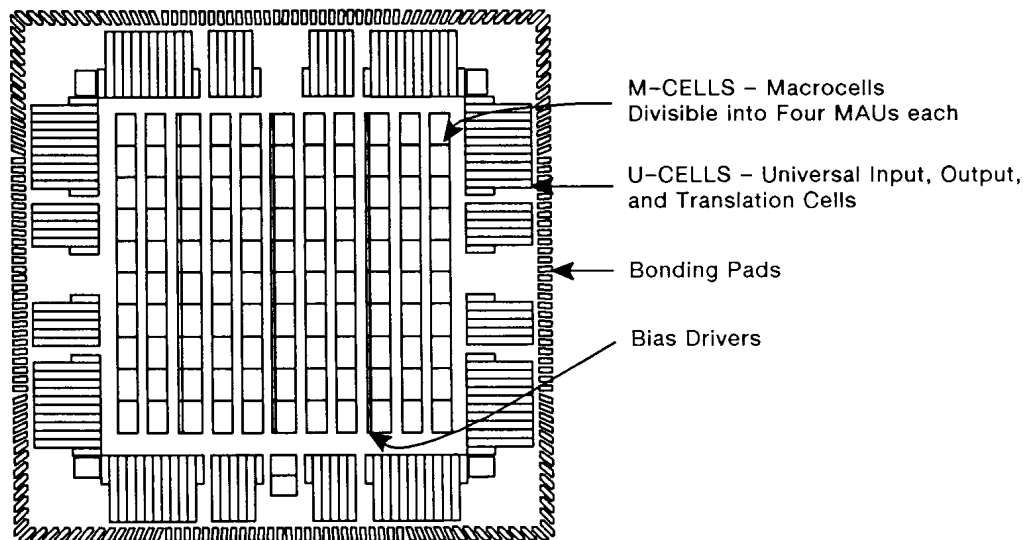
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TABLE 2 – BASIC MCA3 ETL SERIES ARRAY FEATURES

1. Compatible with ECL 100K, 100E, PECL (ECL @ +5.0V), and TTL input/output logic levels
2. Fully programmable I/O cell (U-cell) capable of all compatibility options and translations
3. Macro power from: 1.2 – 2.4mW /2-input OR @ -4.5V
4. Inputs capable of operating at 2.6 GHz; Outputs operational at 1.6 GHz
5. Input cell delays: 200 ps (H macro); 275 ps (L macro) worst case
6. Internal cell delays: 200 ps (H macro); 250 ps (L macro) worst case (2-input OR, FO=1, metal=0)
7. Output cell delays: approx. 350 ps worst case (+ package delay: 100 – 400 ps)
8. TTL input translation delay: 700 ps (H macro); 850 ps (L macro) worst case
9. TTL output translation delay: 2475 ps worst case @ 15pF and 24mA output current
10. Standard and cutoff 50 and 25 ohm ECL output drivers. Optional low-power 60 ohm drivers
11. TTL push pull and tri-state outputs. 12mA and 24mA output current sinks
12. Bidirectional ECL and TTL I/O macros
13. Compatible with FAST™ TTL circuitry
14. Series-Terminated (STECL) outputs with on-chip series resistors and programmable current sinks
15. Expandable MUX/DECODE macro functions
16. Three-level series gated macros available for increased functional density and performance
17. Typical array power: 1-2 Watts for 750ETL; 4-7 Watts for 3200ETL; 7-12 Watts for 6200ETL

FIGURE 2 – MCA3200ETL ARRAY FLOORPLAN EXAMPLE



PRODUCT DESCRIPTION

The MCA3 ETL Series contains three array densities offering the equivalent of 858 to over 6915 gates (see Table 1). The arrays are fabricated using Motorola's MOSAIC III oxide-isolated, poly-electrode-transistor (PET) process (see "PROCESS DESCRIPTION" Section). Unloaded gate delays for the 750, 3200, and 6200 ETL arrays are typically 150 picoseconds for a fanout of 1 and no metal.

The basic array floorplan is illustrated in Figure 2. There are two types of cells: major (M) cells and universal (U) cells. The extensive MCA3 Series macrocell library of internal functions (see "MCA3 ETL MACRO LISTING") can be implemented in the (M) cells. A versatile I/O logic and translator macro selection is available for use in (U) cells. Using this library, the designer can create schematics on a workstation such as the Mentor Graphics® (HP Apollo® Com-

puter). Designs are limited only by the functions in the logic library, and the number of I/O pins on the package.

The majority of the designer's circuit is implemented using internal major (M) cells. Major cells are subdivided into quarter cells which allow up to four different logic circuits to be placed within one M-cell location to achieve maximum array utilization. The internal cells contain a wide variety of SSI/MSI functions ranging from combinational logic to several forms of latches and flip-flops. An internal quarter cell (Minimum Addressable Unit - MAU) can contain functions as large as a D flip-flop (the L882 is a dual D flip-flop in 2 MAU's). Additional logic and level translations may be implemented in the input and output universal (U) cells.

Mixed Mode I/O

ECL or TTL inputs must enter the chip through universal (U) cells. These I/O-cells serve as input buffers as well as performing useful logic functions such as a Latch or a 2-input OR/NOR TTL to ECL translator. Any signal leaving the array must go through a universal (U) cell. Output macros are capable of either logic level translation to TTL or implementing a variety of logic functions such as: Latches, MUXes, and EXOR/EXNORs. Bidirectional macros are placed in one U-cell. Both ECL and TTL Bidirectional macros are available.

The chip uses ECL circuitry for the internal array and ECL/TTL for the I/O. Figure 3 shows the four possible implementations for an ETL array. The I/O system allows the array to be utilized in full ECL, full TTL, PECL/TTL and ECL/TTL (ETL) systems. In ECL environments, either 100K @ -5.2V ± 5%, or 100K @ -4.5V ± 0.3V, may be selected. Outputs are capable of driving 60 ohm, 50 ohm, and 25 ohm loads. Differential I/O are available at a cost of two I/O cells. TTL push pull and tristate outputs are supported, 12mA and 24mA output current sinks can be chosen.

PECL is Pseudo-ECL or positive referenced ECL. This interface operates between 0 and +5.0V rather than the -5.2V or -4.5V for normal ECL. Macro performance is identical to operation at normal ECL levels. PETL stands for Pseudo-ECL

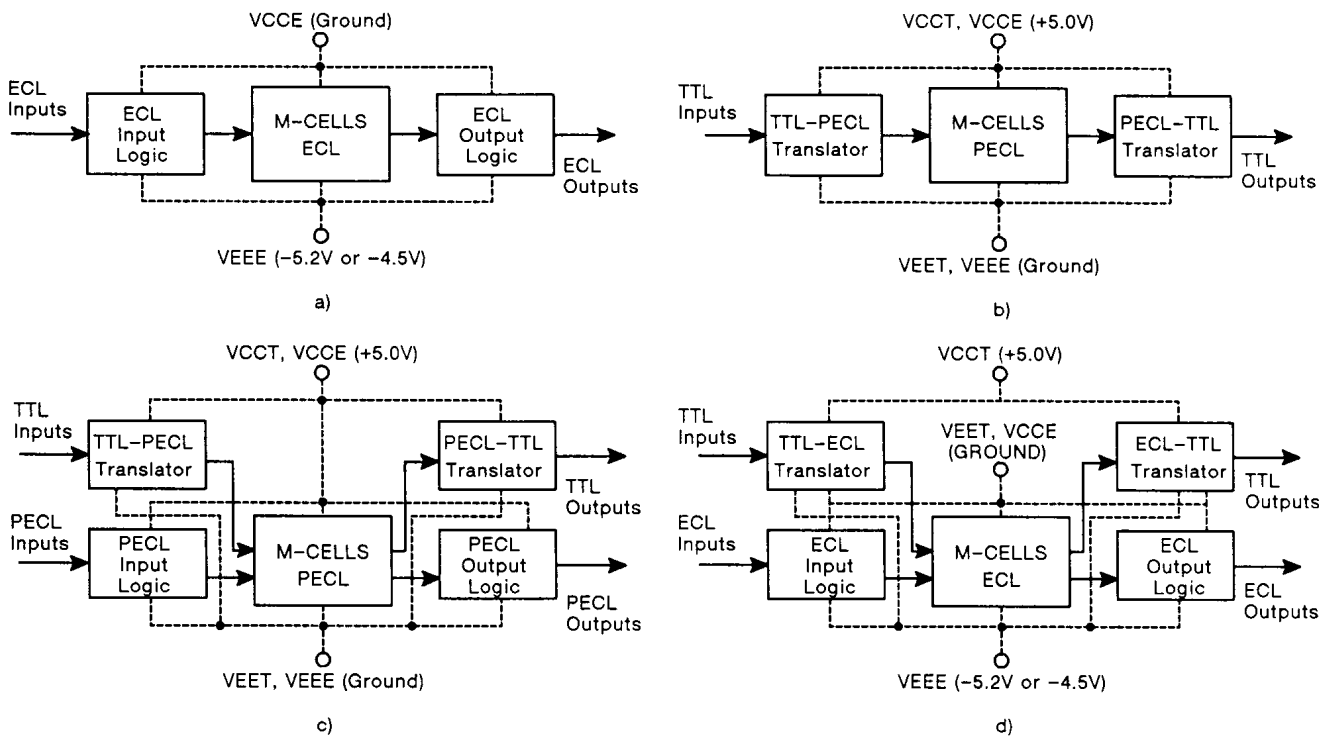
and TTL Levels where TTL translation to PECL on-chip levels is performed. PECL and PETL are used for high performance interfacing in systems with only TTL power supplies available.

Three Layer Metal

The MCA3 ETL Series uses three layers of metal: two layers for internal macro implementation and inter-macro routing, and a third layer for power and ground bussing. Macro interconnection, power, and ground distribution routing are invisible to the user. Vertical (metal-1) channels are located between the columns of cell sites. Horizontal (metal-2) channels may be routed over the macrocell locations. The placement of a macro, therefore, never obstructs metal-2 routing. All metal layers are separated by a layer of dielectric isolation and are connected using "VIA's".

Macros such as adders, multiplexers, decoders, latches, flip-flops, XORs, AND-ORs, etc. are built using first layer metal within a cell. (Horizontal metal-2 routing channels are not required.) This eliminates the majority of interconnects that normally have to be made in the channels of a gate array and significantly reduces routing channel requirements. MCA3 ETL arrays contain a number of free routing channels which is generally sufficient to provide for auto-routability even in an 100% utilized array.

FIGURE 3 — MCA3 ETL ARRAY SIGNAL INTERFACES a)ECL b)TTL c)PECL/TTL d)ECL/TTL



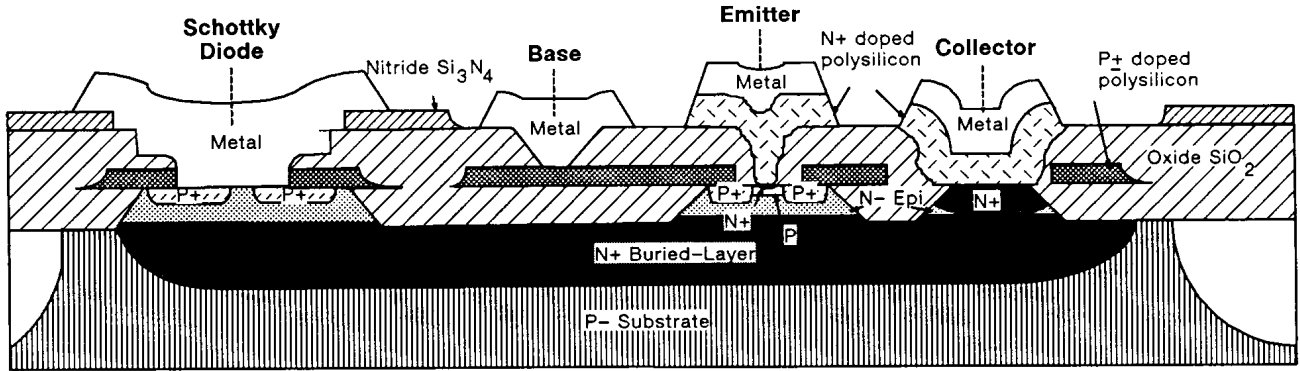
PROCESS DESCRIPTION

The MCA3 Series of arrays is implemented using the process called MOSAIC III which achieves high performance requirements through delivering internal gate delays of 0.15ns (typical) at 0.53mA switch current. This third-generation process is oxide-isolated in the same manner as was its predecessor, MOSAIC II.

The key improvement over MOSAIC II is the use of the poly-electrode-transistor (PET) structure which utilizes p+ polysilicon for extrinsic base doping and the base electrode and n+ polysilicon for the emitter. The polysilicon base electrode greatly enhances switching speed by re-

ducing the series base resistance and collector-base capacitance. An "edge-defined" technique is used to achieve submicron emitter widths without the use of submicron lithography. MOSAIC III allows for polysilicon resistors in order to reduce node capacitance. A Schottky module is incorporated into the standard MOSAIC III process for fabrication of guarded and non-guarded Schottky devices. Figure 4 contains a cross section diagram of a Schottky transistor. With the Schottky module, high performance TTL inputs and outputs are possible.

FIGURE 4 – CROSS SECTION OF MOSAIC III SCHOTTKY TRANSISTOR



DESIGN FEATURES

Universal I/O Structure

The placement of I/O macros within U-cells around the periphery of the array's internal logic permits the chip's interface pins to be programmed as inputs, outputs, or bidirectional I/O. The U-cells also provide the function of ECL, PECL, or TTL logic level translation. Each array contains one U-cell for each available I/O signal pad. The number of I/O signal pads for each array is listed in the table of Array Features on page 1. U-cells contain a number of devices including Schottky transistors and diodes; all TTL output macros are compatible with FAST™ circuitry. The ECL to TTL output translator gate portion of a typical U-cell TTL output macro is schematically represented in Figure 5. The ECL portion of the TTL output macro (not shown) may be a tri-stated, 2-Input OR or NOR gate which is driven from the internal portion of the array.

Operating Frequencies

The input and output frequencies of the array will depend on the I/O macro selected, the package type, and package pin used. Each package contains several pins with minimum distance to the die which allow for maximum frequency operation. In a design, these pins may be selected for critical signals requiring optimum performance. The L/H 7xx Series macros in conjunction with differential input and output macros (C70 and E70) were specifically designed for high frequency applications. Maximum operating frequencies for the MCA3 ETL arrays are shown in Table 3.

FIGURE 5 – TTL OUTPUT STAGE

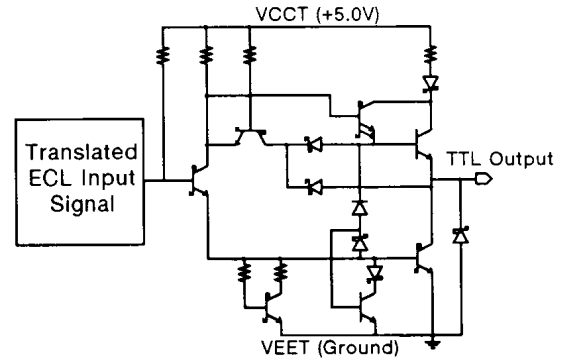


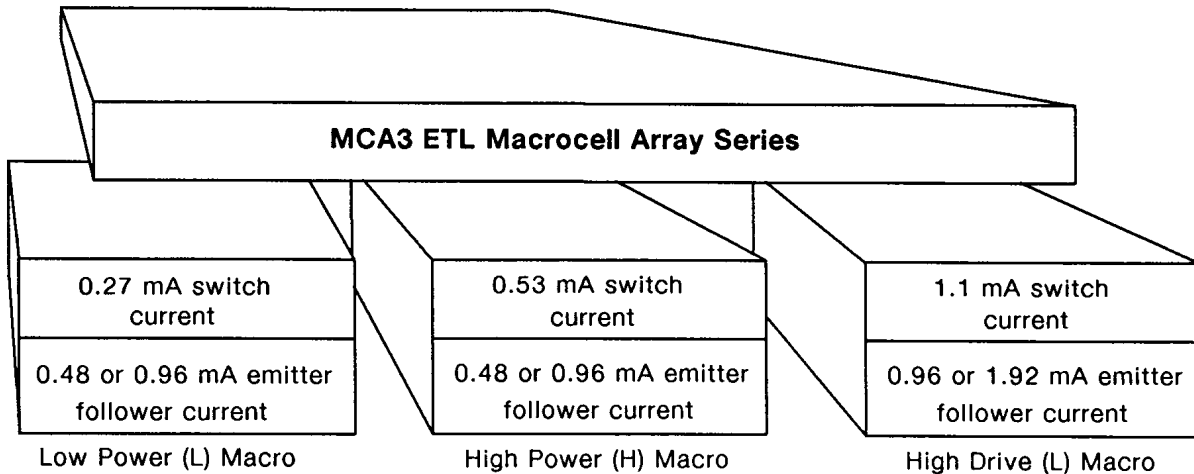
TABLE 3 – ARRAY OPERATING FREQUENCIES

| Signal Type | | Max. Freq. (MHz) | Max. Freq. (MHz) |
|-------------|--------|------------------|------------------|
| | | (50% Duty Cycle) | (50% Duty Cycle) |
| | | Single-ended | Differential |
| ECL/PECL | Input | 2600 (1) | 2600 |
| | Output | 1600 | 1600 |
| TTL | Input | 250 | |
| | Output | 100 (@ 15pF) | |

Notes:

1. Input Frequencies up to 2.6 GHz can be obtained with a sinusoidal AC coupled single-ended input.
2. Refer to the MCA3 ETL Design Manual for maximum frequency requirements and limitations.

FIGURE 6 – MACROCELL (M-CELL) POWER PROGRAMMABILITY



Speed/Power Programmability

The speed/power programmability feature of the MCA3 ETL arrays allows the designer to choose from three M-cell macro performance levels (see Figure 6). This is possible through specifying Low Power (L), High Power (H), or High Drive (L) macros in the design. Current-source switch currents are automatically adjusted according to the macro power level selected. Only specific macros (utilized when macro delay time or fanout are critical factors) are offered in the High Drive (L) version. Note that the (L) associated with High Drive is used for the purpose of macro classification and does not denote low power.

The Internal Macrocell library contains tables which list the various macro input/output delay times based on the power (speed performance) level selected. Macro power selection delivers a performance range for a 2-input OR/NOR gate of 300 ps worst case gate delays at 1.2 mW/gate (L202 Macro @ -4.5V typical) power dissipation for low power macro to 225 ps worst case gate delays at 2.4 mW/gate power dissipation for high power version (H202). Several internal and I/O logic functions and their respective power dissipation are shown in Table 4.

In addition to macro delay performance through macro power level selection, the output emitter-follower currents for each macrocell can be doubled [twinned - via program selection (see Figure 6)] to provide less net delay when driving large fanouts or long lengths of metal. Worst-case performance characteristics for both output emitter-follower (OEF) configurations (single or twin) are provided in Table 5. Adding this macro output fanout and metal delay to the macro input/output delay determines the total delay for the specific path in question.

Output macro delays specified in the library include the output cell to die pad delay and 15pF loads. A delay from the die pad to package pin results in an additional 100 - 400 ps depending on the package and pin selected.

TABLE 4 – TYPICAL POWER DISSIPATION/FUNCTION

| Logic Function | Power (mW) @ -4.5V | Power (mW) @ +5.0V | Power (mW) @ -5.2V |
|-----------------------------|--------------------|--------------------|--------------------|
| 2-Input OR | 1.2/2.4 | 1.3/2.7 | 1.4/2.8 |
| 2-2 OR/EXOR | 1.9/3.0 | 2.1/3.4 | 2.2/3.5 |
| 2-1 Mux W/EN | 1.9/3.0 | 2.1/3.4 | 2.2/3.5 |
| 1 of 4 Dec W/EN | 3.2/5.5 | 3.6/6.1 | 3.7/6.3 |
| Full Adder | 4.8/7.0 | 5.3/7.8 | 5.5/8.1 |
| D Latch W/Rst | 4.1/5.2 | 4.5/5.8 | 4.7/6.0 |
| D Flip-Flop | 7.0/9.3 | 7.8/10.4 | 8.1/10.8 |
| ECL Input buffer | 1.2/2.4 | 1.3/2.7 | 1.4/2.8 |
| ECL Output (2-Input OR) | 15.3/20.2 | 17.0/22.4 | 17.7/23.3 |
| TTL Input Translator (VIH) | 7.0/8.3 | | |
| TTL Output Translator (VOL) | 18.4/34.0 | | |

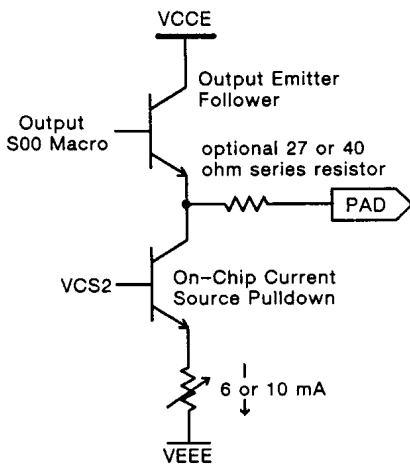
L or H macro switch current is used for respective L/H macro power calculations.

TABLE 5 – INTERNAL MACRO OUTPUT METAL AND FANOUT WORST CASE DELAYS

| OEF Current (power @ -4.5 V) | Macro Type | OEF Delay (ps) | | | |
|--------------------------------------|------------|---------------------------|-----|----------------------------|-----|
| | | F.O. = 2 90 Mils Metal | | F.O. = 4 150 Mils Metal | |
| | | (+) | (-) | (+) | (-) |
| Single Output 0.48 mA (2.2 mW) | L Macro | 340 | 380 | 660 | 720 |
| | H Macro | 150 | 380 | 300 | 730 |
| Twin Output 0.96 mA (4.4 mW) | L Macro | 330 | 180 | 600 | 340 |
| | H Macro | 140 | 180 | 270 | 350 |

Metal is divided equally between 1st and 2nd layers. Fanout is for L macro inputs.

FIGURE 7 - SERIES-TERMINATED ECL (STECL) OUTPUT



Series-Terminated ECL (STECL) Outputs

To facilitate multichip design, the array provides ECL outputs with programmable current-source pulldowns and selectable, on-chip series-terminating resistors. Figure 7 shows the STECL output circuit. The current source pulldown may be programmed to either 6 or 10 mA and a value of 0, 27, or 40 ohms may be selected for the series-termination. This feature is ideal for ap-

plications where hybrid packaging constraints may make external line terminations difficult.

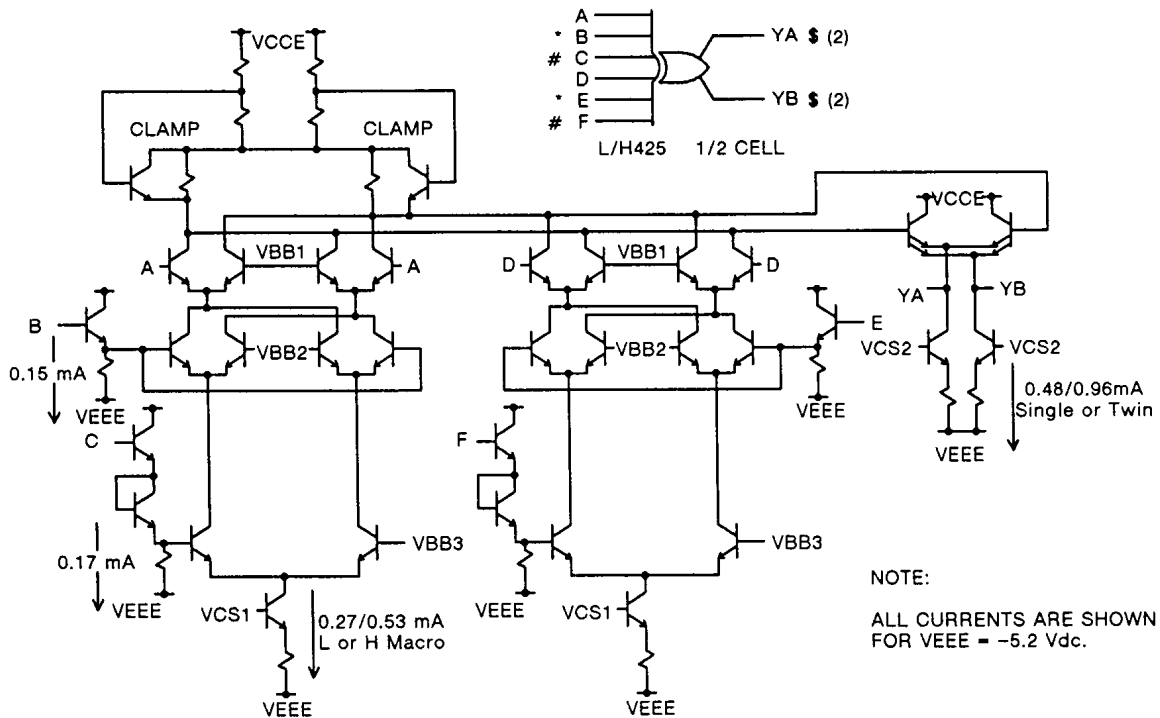
Series Gating

The value of ECL series-gating can be seen in the logic equation for the 6-input exclusive OR gate shown in Figure 8. This EX-OR gate is macro L/H 425 of the M-Cell Library. The second-level inputs into the series-gated tree are indicated by asterisks (*) while the third-level inputs are denoted by pound signs (#).

To implement this function with gates would require thirty-two 6-input AND gates, one 32-input OR gate, and any additional gates required to form the true and complement of each input. If only 3-input gates were used, over one hundred of them would be needed to form the function.

A minimum of 224 connections would be required if gates were used, compared to seven connections for the three-level series gated macro. Each output of the cell has a two-emitter transistor that allows twice the output emitter follower current to be selected for increased drive and performance. The ability to "twin" macrocell outputs allows for output emitter currents of 0.48-0.96 mA. This also provides emitter-dotting (Wired-OR) capability while retaining the non-dotted output function through the second emitter.

FIGURE 8 - SCHEMATIC OF 6-INPUT EXCLUSIVE OR GATE



$$\begin{aligned}
 YA = YB = & \bar{A}BCDEF + A\bar{B}CDEF + ABC\bar{D}EF + ABCD\bar{E}F + ABCDEF + \bar{A}\bar{B}\bar{C}DEF + \bar{A}\bar{B}C\bar{D}EF + \\
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 \end{aligned}$$

DESIGN APPLICATION

One example of an application using high-frequency macros such as H711 is illustrated by the 1.38 GHz Divide By 6 or 7 Counter shown in Figures 9 and 10. The results of the critical path delay calculations from the clock input of the fifth H711 flip-flop to the B data input of the first H711 flip-flop is included on the schematic. If the design requirements demanded higher speed, high-drive flip-flop L714 could have been used in place of the six H711's with a resulting increase in operating frequency to 2.18 GHz. The frequency calculations described above reveal a significant improvement in operating speed for the MOSAIC III technology process used in the MCA3 ETL Series arrays over the MOSAIC II process that provided a 600 MHz

worst-case operating frequency for the same basic circuit design. The differential clock buffer in this example is an L700 macro and the reset buffer is an L202 macro. Note that when the DIV6_7 select line is set high (second portion of timing diagram), OUT 6 stays low after the first clock and the 'divide by 6' circuit function is implemented.

Refer to the Macrocell library included within this data sheet for macro propagation delay times for all macros used in this example.

The designer should be aware that Motorola does not perform high frequency testing on array options. Therefore, the designer is responsible for adhering to the high frequency design guidelines in the MCA3 ETL Series Design Manual.

FIGURE 9 - 1.38 GHz Divide By 6 or 7 Counter

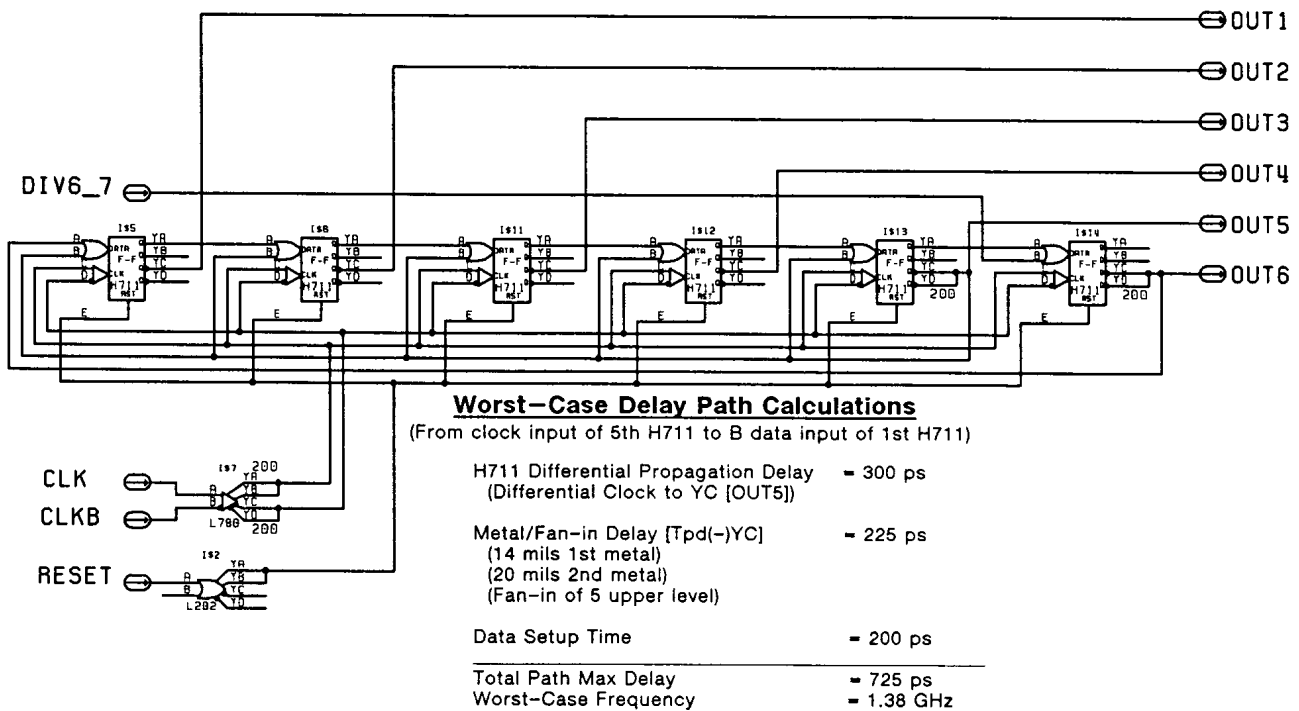
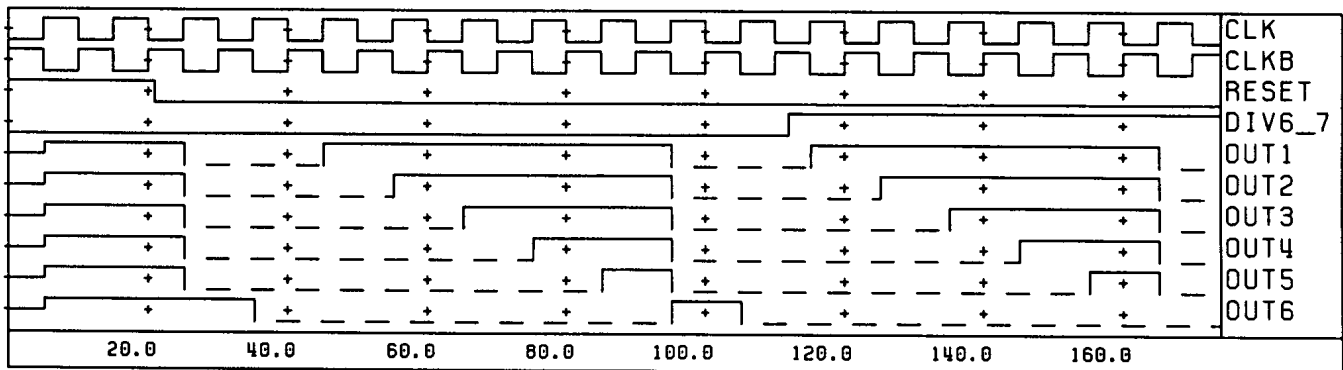


FIGURE 10 - Unit Delay Simulation (QuickSim) of Divide By 6 or 7 Counter



PACKAGING

Primary features of the two Quad Flat Pack (QFP) and two Pin Grid Array (PGA) packages are summarized below. Both the 64 and 160 QFP packages have been designed for optimum high frequency operation by incorporating a strip line characteristic impedance of 50 ohms for the I/O interface. Consult the factory for information concerning the 328 TAB (Tape Automated Bond) version for the MCA6200ETL array. Drawings for each package described below are shown in Figures 18 thru 21.

64 Pin QFP (MCA750ETL):

- 42 I/O
- 22 power/ground
- Plastic (non-hermetic)
- Cu die attach heat slug
- Optional heat sink
- JEDEC registration M0094

160 Pin QFP (MCA3200ETL):

- 120 I/O
- 40 power/ground
- Plastic (non-hermetic)
- Cu die attach heat slug
- Optional heat sink
- JEDEC registration M0108

169 Pin Grid Array (MCA3200ETL):

- 0.100" pin spacing
- 120 I/O
- 49 power/ground
- Multi-layer ceramic (hermetic)
- CuW die attach heat slug
- Wire-bond interconnect
- Ag filled epoxy die attach
- Optional heat sink

224 Pin Grid Array (MCA6200ETL):

- 0.100" pin spacing
- 168 I/O
- 56 power/ground
- Multi-layer ceramic (hermetic)
- CuW die attach heat slug
- Wire-Bond Interconnect
- Ag filled epoxy die attach
- Optional heat sink

Thermal Characteristics Using Heat Sinks

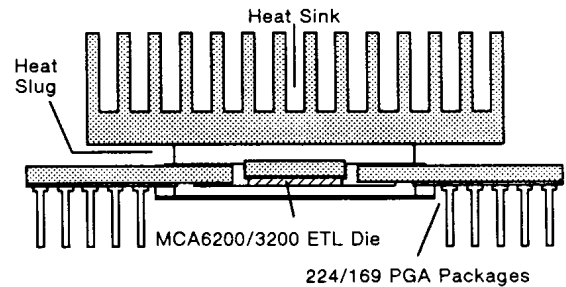
Θ_{JC} , junction to case thermal coefficient, is typically between 1.8 to 2.2°C/W for the 224 and 169 PGA package. Almost all the heat generated by the device is removed via the CuW heat slug to which the die is attached. Therefore, a heat sink or cold plate should be attached directly to the CuW heat slug in order to effectively remove heat from the package and die.

Given that $\Theta_{JA} = \Theta_{JC} + \Theta_{CA}$, the array must operate in a thermal environment such that Θ_{CA} (the thermal resistance between the package case and ambient air) and T_A (the ambient temperature) are controlled in order to meet the T_J specification for AC performance of 115°C.

The heat sinks currently being offered by Motorola for all ETL packages are composed of

black anodized aluminum. For the 224 and 169 PGA packages the heat sink is of the pin-fin type (see Figure 14) and for the 64 and 160 QFP packages is of the circular fin type with a square base (see Figure 15). Figure 11 shows how the heat sink is mounted directly to the heat slug on the package. The chip is also attached directly to the heat slug using a silver filled epoxy compound in order to provide a low thermal resistance. A 'thermal compound' is used between the heat slug and the heat sink to provide good thermal contact. The aluminum heat sinks were chosen because of their overall thermal performance, low cost, and lower weight as compared to copper versions.

FIGURE 11 – Heat Sink Mounted on the 224/169 PGA Packages



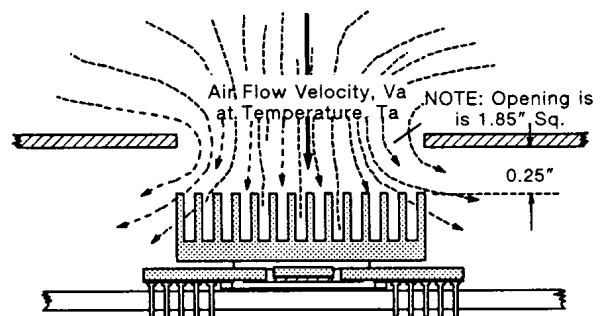
Thermal Test Diode

An option is available on CAD for placing a thermal test diode on an ETL array. When using a test diode, junction temperature and thermal characteristics of the package can be measured by the designer.

Forced Convection Impingement

Forced convection impingement involves forcing ambient air through an opening directly down on the heat sink (see Figure 12). The air flow through the pin fins is generally non-laminar. The thermal resistance from the device to the ambient air (Θ_{JA}) depends heavily on the flow rate of the impinged air.

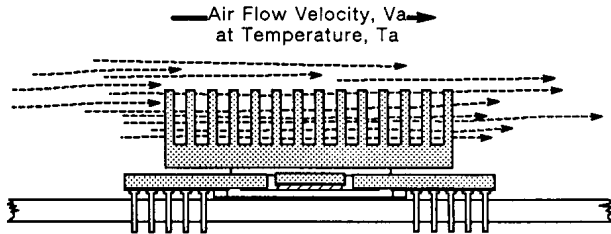
FIGURE 12 – Forced Convection Impingement



**Forced Convection Horizontal
("Conventional Flow")**

Horizontal air flow, or forced convection horizontal is a conventional air flow configuration used in many TTL and lower power ECL environments (see Figure 13). Ambient air is blown horizontally (parallel to the plane of the package) over the package and heat sink.

FIGURE 13 – Forced Convection Horizontal



Heat Sinks and Cooling Considerations

The worst case propagation delays in the MCA3 series macro library are specified for a maximum junction temperature of 115°C. The ECL DC I/O logic levels are specified over a junction temperature range of 25 to 115°C for the 100K interface. The TTL DC I/O logic levels are also specified for junction temperatures over a range of 25 to 115°C.

Figure 16 shows typical package thermal characteristics as a function of air flow. The curves are based on the 224 and 169 PGA packages with an Aluminum pin-fin heat sink attached (see Figure 14). The heat sink was attached using a Hi-thermal conduction adhesive applied approximately 0.004 inch thick on the heat sink. Pressure was applied to remove bubbles and insure proper mating. The adhesive was cured at 150°C for 30 minutes. Figure 17 shows the same type of package thermal characteristic curves for the 64 and 160 QFP packages.

The thermal requirements for an MCA3 ETL design will vary according to array size, percent utilization of the array, desired reliability levels, and the mixture of high and low power macrocells within the array. The MCA6200ETL array (7-12 Watts-typical) and the MCA3200ETL array (4-7 Watts-typical) power dissipation for a fully utilized chip requires a heat sink with air flow to meet the maximum junction temperature limit of 115°C for AC specifications. For the MCA750ETL (1-2 Watts-typical), a heat sink may be required depending on ambient temperature and power dissipation.

FIGURE 14 – Aluminum Pin-Fin Heat Sink for 224/169 PGA Packages (Thermalloy #2329B)

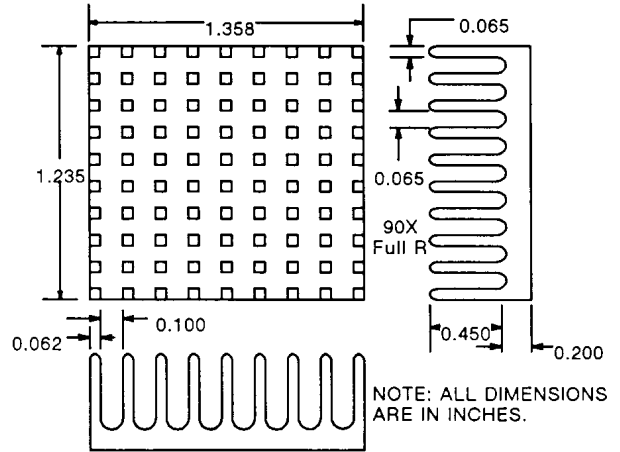
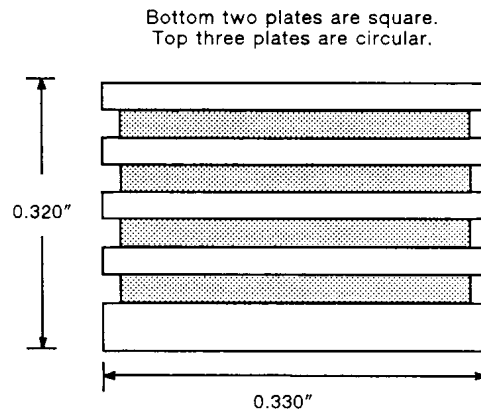


FIGURE 15 – Aluminum Circular Fin Heat Sink for 64 QFP Package (Motorola H00809A001)



Thermal Resistance

The total thermal resistance of the packaging configuration depends on many variables including parallel heat flow paths other than from the die to the heat sink (e.g. heat may flow from the board itself to the heat sink.) The thermal resistance from the die to the heat sink is composed of thermal resistances for the silicon, epoxy die attach, and the heat sink.

Thermal Calculations

The modest power requirements for the ETL arrays combined with good package thermal characteristics should minimize any thermal problems. Junction temperature can be calculated with the equation:

$$T_J = T_A + P_D \Theta_{JA}$$

where

- T_J = Junction temperature
- Θ_{JA} = Thermal coefficient (from Figure 16)
- P_D = Array power dissipation
- T_A = Ambient temperature

For example, based on the following list of assumptions, the junction temperature can be calculated as follows:

Assumptions:

- 224 PGA with heat sink
- $T_A = 50^\circ\text{C}$ (ambient)
- $P_D = 11$ Watts (die power)
- air flow = 500 lfpm

From Figure 16, $\Theta_{JA} = 3.1^\circ\text{C/W}$

The junction temperature of the device is given by:

$$T_J = T_A + P_D \Theta_{JA} = 50 + (11)(3.1) = 84.1^\circ\text{C}$$

This number is well below the 115°C specified maximum junction temperature for the array.

64 QFP Thermal Considerations

Based on similar calculations as for the 224 PGA, a 64 QFP dissipating 1.5 watts with no heat sink can be used in ambient temperatures up to 68.5°C before reaching the maximum junction temperature of 115°C . While still dissipating 1.5 watts but with a heat sink and 200 lfpm of air flow, the 64 QFP can be used in ambient temperatures up to 91°C . Dissipating 2.0 watts with a heat sink and 500 lfpm of air flow, the 64 QFP can be used in ambient temperatures up to 94°C .

FIGURE 16 – Thermal Resistance 169 and 224 PGAs (Typical)

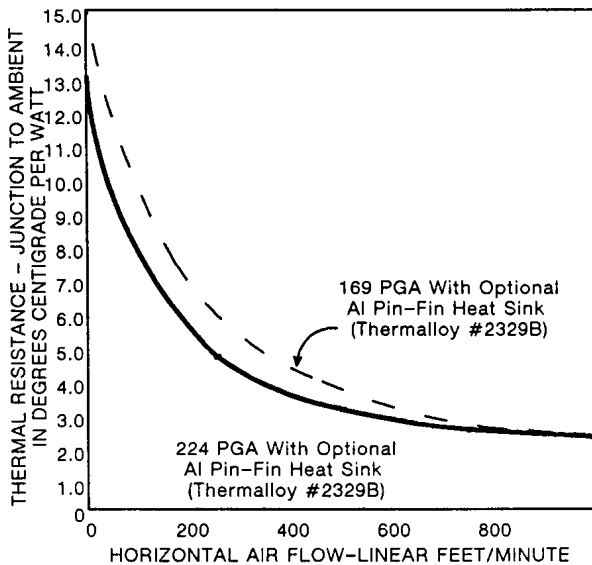


FIGURE 17 – Thermal Resistance 64 and 160 QFPs (Typical)

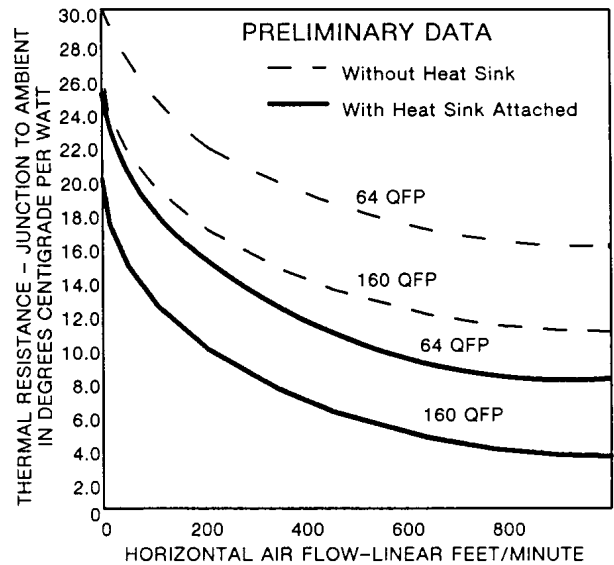
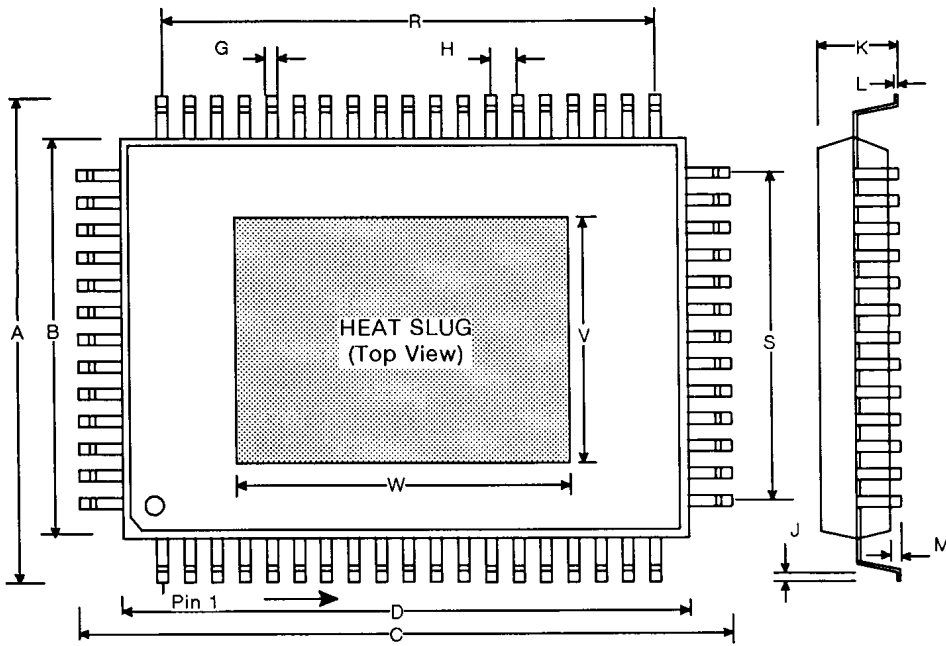
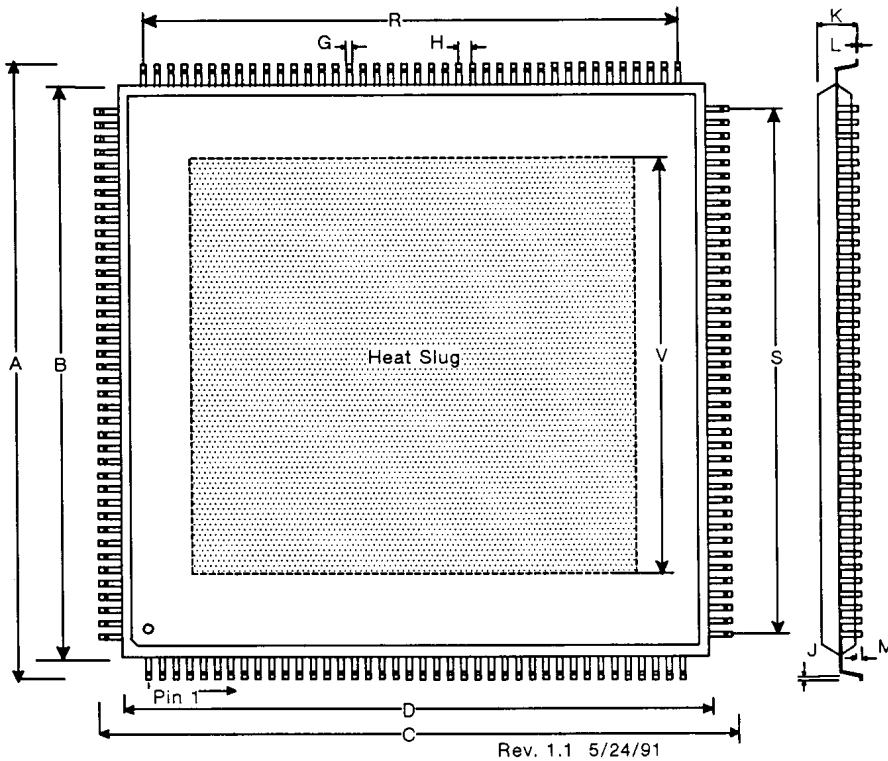


FIGURE 18 — 64 QFP PACKAGE



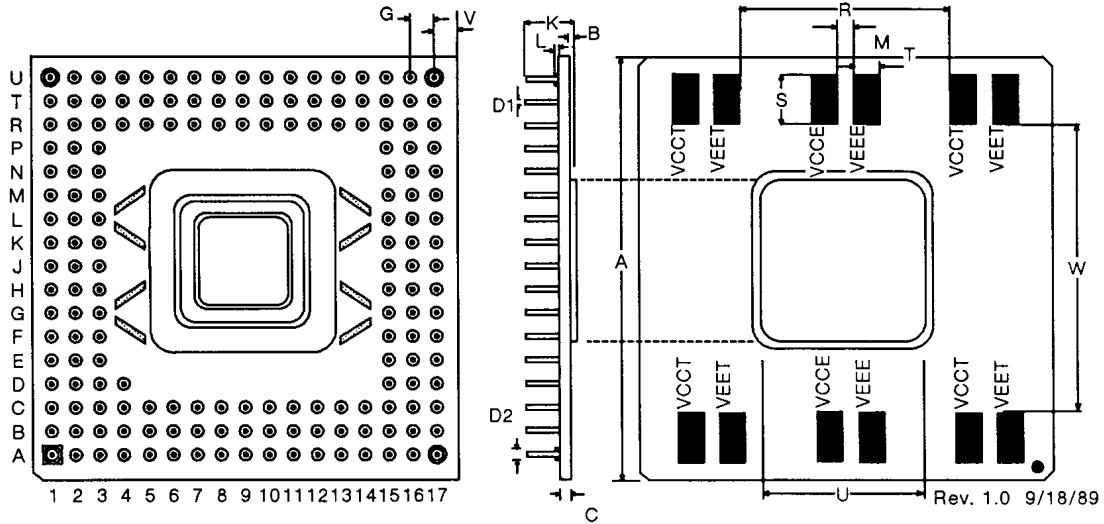
| DIM | MILLIMETERS | |
|-----|-------------|-------|
| | MIN | MAX |
| A | 17.10 | 17.37 |
| B | 13.90 | 14.10 |
| C | 23.10 | 23.37 |
| D | 19.90 | 20.10 |
| G | 0.381 | 0.559 |
| H | 1.000 TYP. | |
| J | 0.75 | 0.92 |
| K | 2.85 | 3.15 |
| L | 0.10 | 0.18 |
| M | 0.25 | 0.35 |
| R | 18.0 Ref. | |
| S | 12.0 Ref. | |
| V | 8.8 TYP. | |
| W | 11.5 TYP. | |

FIGURE 19 — MCA3200ETL 160 QFP (Preliminary)



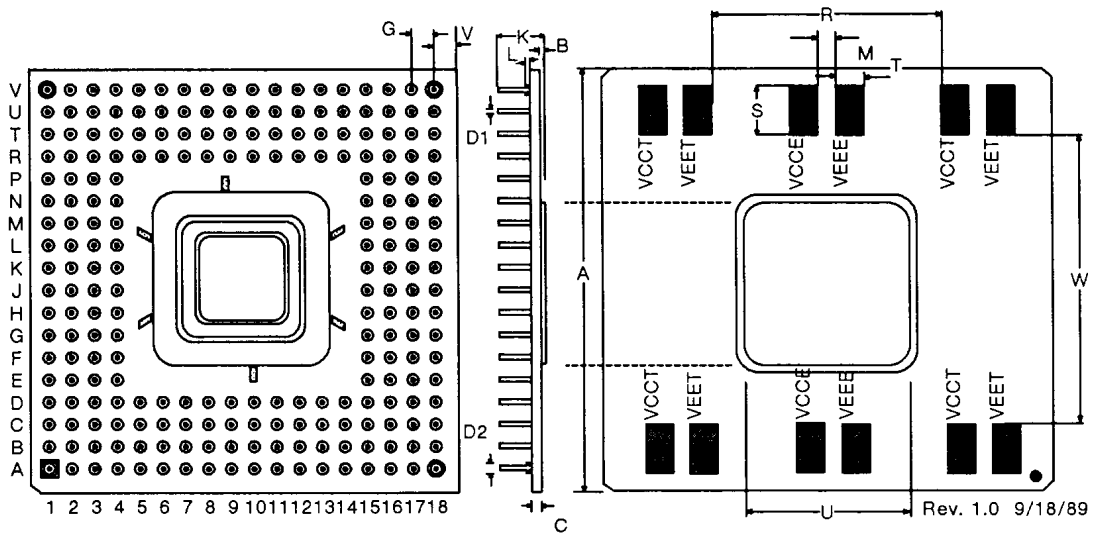
| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|-------|------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 31.10 | 31.37 | 1.224 | 1.235 |
| B | 27.90 | 28.10 | 1.098 | 1.106 |
| C | 31.10 | 31.37 | 1.224 | 1.235 |
| D | 27.90 | 28.10 | 1.098 | 1.106 |
| G | 0.220 | 0.380 | 0.009 | 0.015 |
| H | .650 BSC | | 0.0256 BSC | |
| J | 0.75 | 0.92 | 0.030 | 0.036 |
| K | 3.45 | 3.85 | 0.136 | 0.152 |
| L | 0.13 | 0.18 | 0.005 | 0.007 |
| M | 0.25 | 0.35 | 0.010 | 0.012 |
| R | 25.35 Ref. | | 0.998 Ref. | |
| S | 25.35 Ref. | | 0.998 Ref. | |
| V | 16.8 Sq | | 0.661 | |

FIGURE 20 - 169 PIN GRID ARRAY PACKAGE



| DIM | INCHES | TOLERANCE | DIM | INCHES | TOLERANCE |
|-----|-----------|-----------|-----|--------|-----------|
| A | 1.760 Sq | ±.018 | M | 0.040 | ±.005 |
| B | 0.035 | ±.005 | R | 1.130 | ±.012 |
| C | 0.110 | ±.011 | S | 0.120 | ±.005 |
| D1 | 0.018 DIA | ±.001 | T | 0.060 | ±.005 |
| D2 | 0.050 DIA | ±.005 | V | 0.080 | ±.005 |
| G | 0.100 | ±.005 | U | 0.700 | ±.009 |
| K | 0.325 | ±.005 | W | 1.420 | ±.014 |
| L | 0.050 | ±.005 | | | |

FIGURE 21 - 224 PIN GRID ARRAY PACKAGE



| DIM | INCHES | TOLERANCE | DIM | INCHES | TOLERANCE |
|-----|-----------|-----------|-----|--------|-----------|
| A | 1.860 Sq | ±.019 | M | 0.040 | ±.005 |
| B | 0.035 | ±.005 | R | 1.200 | ±.012 |
| C | 0.110 | ±.010 | S | 0.120 | ±.005 |
| D1 | 0.018 DIA | ±.001 | T | 0.060 | ±.005 |
| D2 | 0.050 DIA | ±.005 | V | 0.080 | ±.005 |
| G | 0.100 | ±.005 | U | 0.750 | ±.008 |
| K | 0.325 | ±.005 | W | 1.520 | ±.015 |
| L | 0.050 | ±.005 | | | |

APPLICATION DESIGN DEVELOPMENT

The first step towards successful design on an MCA3 ETL array is to contact the local Motorola sales office. The sales engineer will describe the array pricing structure and place the customer in contact with a bipolar product marketing specialist. The application is reviewed to assure performance objectives can be met. Design flow variables and program schedules will be explained.

A variety of working relationships can be established between the customer and Motorola. These arrangements may range from a complete Motorola turn-key design effort to the customer doing the schematic, along with pre- and post-layout timing simulation. Customers can perform their own schematic capture and simulation using a Mentor Graphics (HP Apollo) engineering workstation. Motorola provides a workstation based design system for pre- and post-layout simulation to verify design implementation before releasing options to manufacturing.

Once the optimum design flow has been determined, a Semicustom Purchase Agreement (SPA) between the customer and Motorola can be prepared. A SPA specifies the cost to the customer for services in design development and manufacture of prototype devices. The completion of this agreement is normally accomplished when

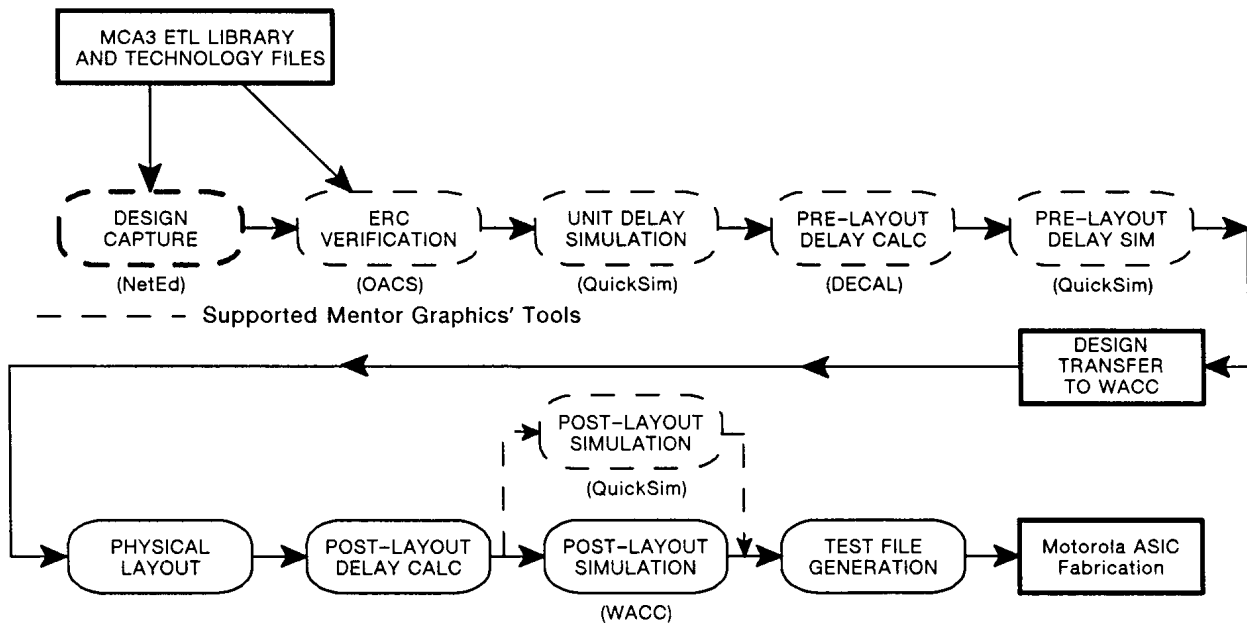
the customer receives fully tested prototype devices.

WORKSTATION/MAINFRAME INTERFACE

Motorola's Open Architecture CAD System (OACS™) supports front end design along with pre- and post-layout timing simulation on Mentor Graphics engineering workstations. Physical layout (place and route) and timing analysis design tools are supported on Motorola's mainframe CAD system (WACC).

In a typical design flow using the MCA3 OACS tool set (see Figure 22), the customer executes the first design phase by developing the schematic (using NetEd™) and performing functional and pre-layout simulations (using QuickSim™) on the workstation. Pre-layout simulations use worst-case macro propagation delays with typical metal lengths per fanout and include worst-case net delays. Motorola then uses the resulting design files to perform physical layout of the circuit on WACC. The post-layout timing files, based on actual wire routing lengths, that originated on WACC are back-annotated to the customer to support QuickSim for final system timing simulations. Design and/or layout iterations are made if necessary. Following a successful post-layout design verification and sign off by the customer, Motorola implements manufacturing the customer's specific ASIC design.

FIGURE 22 — TYPICAL MCA3 ETL OACS SYSTEM DESIGN FLOW



MCA3 OACS 2.0 System Features

- Installation and Verification Utilities
- Produces EDIF 2.0.0 Netlist
- Electrical Rules Checking
- Unit Delay (Functional) Simulation
- Pre- and Post-Layout Simulation

NedEd and QuickSim are Trademarks of Mentor Graphics Corp.

PRODUCT RELIABILITY

The highest possible level of quality in concrete, measurable terms is Motorola's goal for its products and services. Each process and product is extensively characterized and qualified. Reliability assurance engineers work closely with macrocell array designers and computer aided design software engineers to identify and eliminate problem causes. Statistical process control techniques are used in each step of manufacturing to assure first pass design success for all customers.

In addition to initial qualification the Reliability Engineering Department performs ongoing reliability testing to maintain a high level of confidence in fabrication and assembly operations. Failure rates as a function of junction temperature are plotted for the MCA3 ETL arrays in Figure 23. At a junction temperature of 115°C the failure rate is estimated to be: 250 FIT for the 6200ETL; 145 FIT for the 3200ETL; and 50 FIT for the 750ETL

array. An activation energy of 0.70 EV was used to calculate acceleration factors for other temperatures.

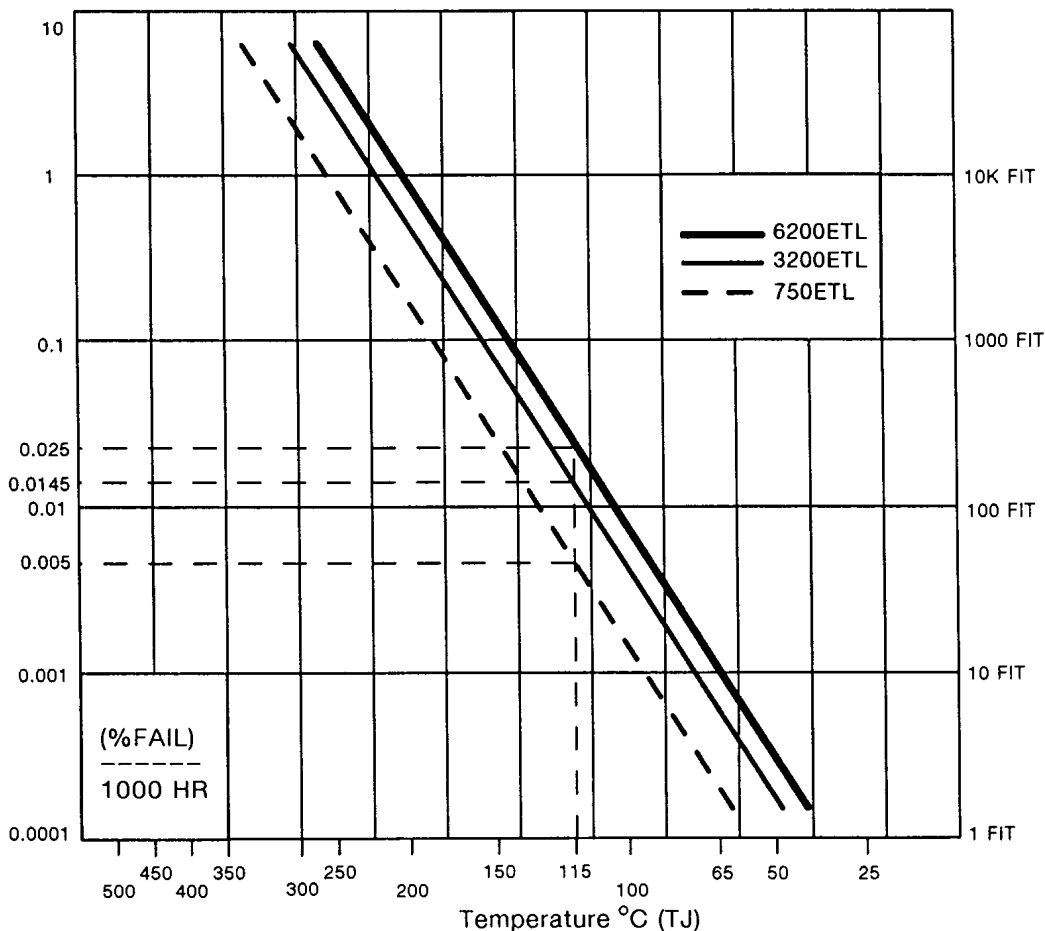
1 FIT = One device failure per 10^9 device hours
or

One part per million failure rate per 10^3 hours

The reliability estimate is based on modeling of various failure mechanisms where the MCA3 ETL arrays features have been compared to other MCA3 arrays as well as previous generation arrays. Comparison of actual reliability data to previous estimates derived in an identical manner have closely predicted actual results.

As a result of exceedingly high quality and reliability standards, Motorola has achieved one of the lowest part reject records in the industry.

FIGURE 23 - FAILURE RATE vs RECIPROCAL TEMPERATURE FOR MCA3 ETL ARRAYS



Estimated static operation average failure-rate as a function of junction temperature
(Slope of line based on Arrhenius equation with 0.70 EV activation energy)

MACROCELL LIBRARY

Each macrocell array M and U Cell location contains a number of conventional transistors and resistors that can be interconnected with CAD selected metal patterns to form logic functions. The macrocell library contains pre-defined metal patterns for more than 180 different logic functions. Designers may select any of the macrocell functions for any M or U Cell site location. Each macrocell, however, may only be placed in the appropriate cell location type. Internal logic functions are placed in M cell locations. Input, output, and translation logic functions for signals going on and off the chip are performed in U cell locations. A listing of all MCA3 ETL macros begins on page 19. Selected examples of I/O and internal macros from the macrocell library are illustrated on pages 15 thru 19.

Worst-case propagation delay is specified for a maximum junction temperature of $T_J \text{ max} = 115^\circ\text{C}$ and worst-case voltage for that particular macro. In general, a lower junction temperature can result in faster propagation delays. ECL/PECL macrocell power dissipation is specified at $V_{EE} = -5.2 \text{ V}$.

The worst-case setup times and minimum pulse widths are specified for all flip-flops and latches. Hold times are zero unless otherwise specified.

An asterisk (*) indicates an input into the 2nd level of a series-gated tree. A pound sign (#) indicates an input into the 3rd level of a series gate structure. Internal input followers are used to translate to the proper levels. Numbers in parentheses in front of inputs indicate DC loading factors for low and high power macros.

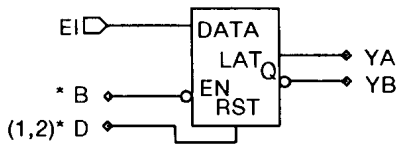
I/O and Translation (U) Cells

Universal cells capable of input, output, and translation are placed around the periphery of the chip. All inputs coming onto the chip must be connected to an input macro. Even when logic level translation is not required, U-cells are necessary to ensure full compatibility and adequate noise margins when interfacing with the various ECL logic families. Interface cells can perform TTL to ECL/PECL translation combined with several logic functions. ECL/PECL output macros are used primarily to provide an output interface between the internal logic in the array and the logic outside the package by supplying 25 ohm, 50 ohm, and 60 ohm drive capability. Output and bidirectional macros also provide the logic functions of OR-AND, EXORs, and latches in addition to logic level translation.

SELECTED MACROCELL EXAMPLES

ECL/PECL INPUT MACROS

MACRO: C50 INPUT LATCH with ENABLE LOW
1 U-CELL
2 LEVEL SERIES GATING



POWER: (mW)

L Macro 8.6

H Macro 9.9

TRUTH TABLE

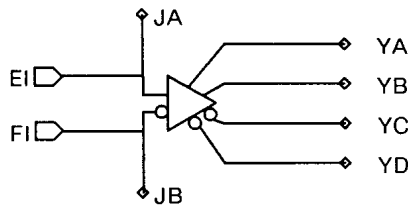
| RST | DATA | ENABLE | Q |
|-----|------|--------|----|
| D | EI | B | YA |
| H | X | H | L |
| L | X | H | -- |
| X | L | L | L |
| X | H | L | H |

NOTE: -- = NO CHANGE

| MACRO DELAYS (ps) | | L MACRO | | H MACRO | |
|-----------------------|--------|---------|-----|---------|-----|
| IN | OUT | (+) | (-) | (+) | (-) |
| EI | YA, YB | 400 | 400 | 250 | 250 |
| B | YA, YB | 425 | 525 | 300 | 350 |
| D | YA | -- | 525 | -- | 375 |
| D | YB | 525 | -- | 375 | -- |
| SET UP | | 600 | | 450 | |
| Min CLOCK PULSE WIDTH | | 1000 | | 750 | |
| Min RESET PULSE WIDTH | | 1075 | | 825 | |

MACRO: C70 DIFFERENTIAL INPUT BUFFER WITH OFF CHIP TERMINATION INPUTS
HI DRIVE MACRO

2 U-CELLS
1 LEVEL SERIES GATING



POWER: (mW)

L Macro 7.8

| MACRO DELAYS (ps) | | L MACRO | | H MACRO | |
|-------------------|----------------|---------|-----|---------|-----|
| IN | OUT | (+) | (-) | (+) | (-) |
| EI, FI | YA, YB, YC, YD | 75 | 100 | | |

TRUTH TABLE

| EI | FI | YA, YB | YC, YD |
|----|----|--------|--------|
| L | L | ND | ND |
| L | H | L | H |
| H | L | H | L |
| H | H | ND | ND |

NOTE: ND = NOT DEFINED

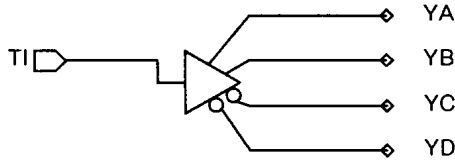
NOTES:

Outputs JA and JB can be used as off-chip input termination ports when connected via Macro E75. If outputs JA and JB are left open, Macro C70 may be used as a standard differential input buffer.

SELECTED MACROCELL EXAMPLES

TTL TO ECL INPUT TRANSLATOR MACRO

MACRO: T00 TRANSLATOR
With True and Complement
 1 U-CELL
 1 LEVEL SERIES GATING



| Power (mW) | L MACRO | H MACRO |
|-------------------|---------|---------|
| VCCT (Input High) | 2.6 | 2.6 |
| VCCT (Input Low) | 1.8 | 1.8 |
| VEEE | 4.4 | 5.7 |

| MACRO DELAYS (ps) | | L MACRO | | H MACRO | |
|-------------------|-------|---------|-----|---------|-----|
| IN | OUT | (+) | (-) | (+) | (-) |
| TI | YA,YB | 625 | 850 | 575 | 700 |
| TI | YC,YD | 750 | 700 | 600 | 650 |

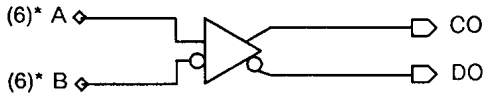
$$TI = YA = YB = \overline{YC} = \overline{YD}$$

ECL/PECL OUTPUT MACROS

NOTE:

DC loading is shown in parentheses (). For example, if (8,12) is shown, that input represents a DC load of 8 for a low power macro and 12 for a high power macro. The number of AC loads is shown in a separate table if it is other than one. Output macro specifications include metal routing, die pad, and package capacitive loading effects.

MACRO: E70 DIFFERENTIAL OUTPUT BUFFER
 2 U-CELLS
 1 LEVEL SERIES GATING



$$CO = \overline{DO} = A = \overline{B}$$

NOTES:

Inputs A and B should be treated as upper level inputs for AC and DC fan-in considerations only. These inputs follow the I/O connection rules for second level inputs.

POWER: (mW)
 H Macro 57.2

| MACRO DELAYS (ps) | | L MACRO | | H MACRO | |
|-------------------|-------|---------|-----|---------|-----|
| IN | OUT | (+) | (-) | (+) | (-) |
| A,B | CO,DO | | | 150 | 225 |

TRUTH TABLE

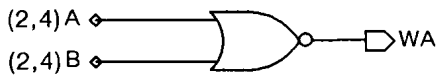
| A | B | DO | CO |
|---|---|----|----|
| L | L | ND | ND |
| L | H | H | L |
| H | L | L | H |
| H | H | ND | ND |

NOTE: ND = NOT DEFINED

| NUMBER OF AC LOADS | | | |
|--------------------|-----------|-----------|-----------|
| INPUT | 1st LEVEL | 2nd LEVEL | 3rd LEVEL |
| A,B | | 2 | |

ECL TO TTL OUTPUT TRANSLATOR MACROS

MACRO: T30 NOR TRANSLATOR
 1 U-CELL
 1 LEVEL SERIES GATING



$$\overline{WA} = A + B$$

| Power (mW) | L MACRO | H MACRO |
|--------------------|---------|---------|
| VCCT (Output Low) | 14.8 | 27.0 |
| VCCT (Output High) | 5.8 | 8.9 |
| VEEE | 3.6 | 7.0 |

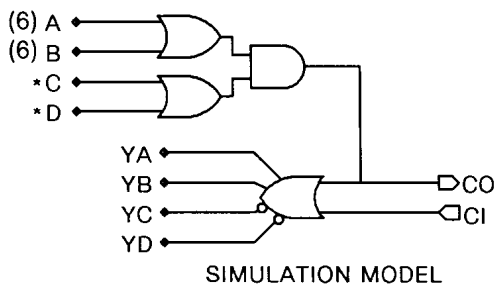
| MACRO DELAYS (ps) | | L MACRO | | H MACRO | |
|---------------------|-----|---------|------|---------|------|
| IN | OUT | (+) | (-) | (+) | (-) |
| A,B | WA | 2875 | 3450 | 2475 | 2275 |
| Load Factor (ps/pF) | | 35 | 44 | 19 | 39 |

Use Load Factor to determine the delay for external loading.

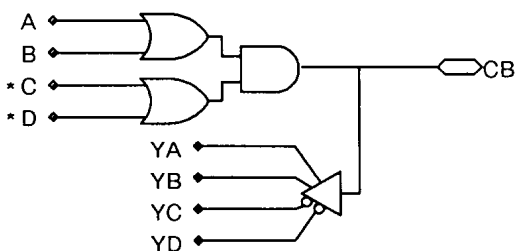
SELECTED MACROCELL EXAMPLES

BIDIRECTIONAL I/O MACROS

MACRO: B26 2-2 OR/AND
 With Input Buffer (50 ohm output)
 1 U-CELL
 2 LEVEL SERIES GATING



SIMULATION MODEL

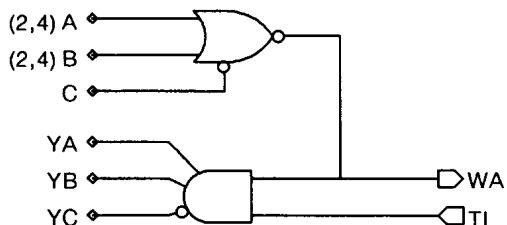


POWER: (mW)
 H Macro 20.6

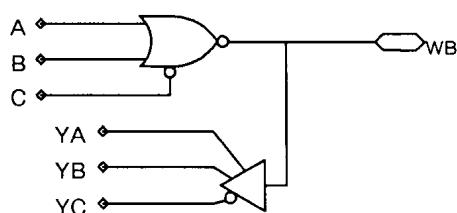
| MACRO DELAYS (ps) | | L MACRO | | H MACRO | |
|-------------------|-------|---------|-----|---------|-----|
| IN | OUT | (+) | (-) | (+) | (-) |
| A,B | CB | | | 375 | 300 |
| A,B | YA,YB | | | 550 | 500 |
| A,B | YC,YD | | | 425 | 550 |
| C,D | CB | | | 425 | 350 |
| C,D | YA,YB | | | 600 | 550 |
| C,D | YC,YD | | | 475 | 600 |
| CB | YA,YB | | | 175 | 200 |
| CB | YC,YD | | | 125 | 175 |

$$CB = YA = YB = \overline{YC} = \overline{YD} = (A+B) \cdot (C+D)$$

MACRO: T64 ECL 2-INPUT NOR TRANSLATOR and TTL to ECL INPUT BUFFER
 With ECL Tri-State Enable
 1 U-CELL
 1 LEVEL SERIES GATING



SIMULATION MODEL



| Power (mW) | L MACRO | H MACRO |
|-----------------|---------|---------|
| TOTAL (WB Low) | 46.7 | 65.7 |
| TOTAL (WB High) | 39.5 | 50.0 |
| TOTAL (WB ZH) | 49.6 | 70.2 |
| TOTAL (WB ZL) | 48.8 | 69.4 |

| MACRO DELAYS (ps) | | L MACRO | | | | H MACRO | | | |
|---------------------|-------|---------|------|------|------|---------|------|------|------|
| IN | OUT | (+) | (-) | (+) | (-) | (+) | (-) | (+) | (-) |
| A,B | WB | 2950 | 3625 | 2575 | 2400 | | | | |
| A,B | YA,YB | 3575 | 4475 | 3150 | 3100 | | | | |
| A,B | YC | 4375 | 3650 | 3000 | 3250 | | | | |
| Load Factor (ps/pF) | | 43 | 36 | 39 | 19 | | | | |
| | | ZH | ZL | HZ | LZ | ZH | ZL | HZ | LZ |
| C | WB | 2650 | 4500 | 3400 | 2375 | 2550 | 2900 | 2825 | 2300 |
| Load Factor (ps/pF) | | 46 | 66 | 59 | 25 | 43 | 30 | 65 | 30 |
| WB | YA,YB | 625 | 850 | 575 | 700 | | | | |
| WB | YC | 750 | 700 | 600 | 675 | | | | |

Macro delays are for 15pF. Use Load Factor to determine the delay for other loads.

TRUTH TABLE

| A | B | C | WB | YA,YB | YC |
|---|---|---|----|-------|----|
| X | X | H | Z | X | X |
| L | L | L | H | H | L |
| H | X | L | L | L | H |
| X | H | L | L | L | H |
| X | X | H | L | L | H |
| X | X | H | H | H | L |

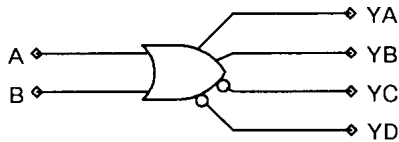
SELECTED MACROCELL EXAMPLES

INTERNAL MACROS

The M Cells in the array comprise the internal area on the chip and are used for the majority of logic capability. The macros in the Internal M-Cell library use 1/4, 1/2, 3/4 or 1 entire cell

location. Each macro specifies how much of the cell is needed to implement that particular function.

MACRO: 202 2-Input OR/NOR
1/4 CELL
1 LEVEL SERIES GATING



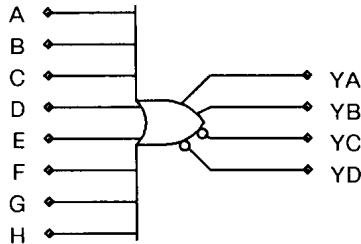
POWER: (mW)

L Macro 1.4 H Macro 2.8

| MACRO DELAYS (ps) | | L MACRO | | H MACRO | |
|-------------------|-------|---------|-----|---------|-----|
| IN | OUT | (+) | (-) | (+) | (-) |
| A,B | YA,YB | 250 | 250 | 200 | 200 |
| A,B | YC,YD | 250 | 300 | 200 | 225 |

$$YA = YB = \overline{YC} = \overline{YD} = A + B$$

MACRO: 403 8-INPUT OR/NOR
1/4 CELL
1 LEVEL SERIES GATING



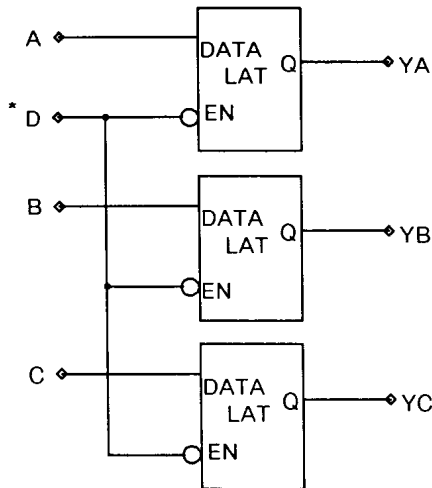
POWER: (mW)

L Macro 1.4 H Macro 2.8

| MACRO DELAYS (ps) | | L MACRO | | H MACRO | |
|-------------------|-------|---------|-----|---------|-----|
| IN | OUT | (+) | (-) | (+) | (-) |
| A,B,C,D,E,F,G,H | YA,YB | 225 | 250 | 175 | 200 |
| A,B,C,D,E,F,G,H | YC,YD | 800 | 725 | 475 | 400 |

$$YA = YB = \overline{YC} = \overline{YD} = A + B + C + D + E + F + G + H$$

MACRO: 893 3xD LATCH WITH COMMON CLOCK
1/2 CELL
2 LEVEL SERIES GATING



POWER: (mW)

L Macro 12.8

| MACRO DELAYS (ps) | | L MACRO | | H MACRO | |
|------------------------|----------|---------|-----|---------|-----|
| IN | OUT | (+) | (-) | (+) | (-) |
| A,B,C | YA,YB,YC | 350 | 400 | | |
| D | YA,YB,YC | 475 | 525 | | |
| SET UP TIME | | 600 | | | |
| MIN ENABLE PULSE WIDTH | | 1000 | | | |

TRUTH TABLE

| DATA | EN | Q |
|-------|----|----------|
| A/B/C | D | YA/YB/YC |
| X | H | -- |
| L | L | L |
| H | L | H |

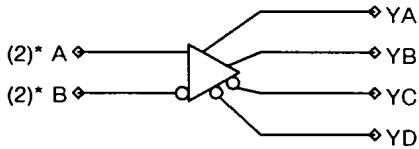
NOTE: -- = NO CHANGE

NOTE:
Latches are enabled when input D is low.

SELECTED MACROCELL EXAMPLES

DIFFERENTIAL INTERNAL (M) CELLS

**MACRO: 700 DIFFERENTIAL LINE RECEIVER
HI DRIVE MACRO**
1/2 CELL
1 LEVEL SERIES GATING



POWER: (mW)
L Macro 10.6

| MACRO DELAYS (ps) | | L MACRO | | H MACRO | |
|-------------------|-------|---------|-----|---------|-----|
| IN | OUT | (+) | (-) | (+) | (-) |
| A,B | YA,YB | 125 | 125 | | |
| A,B | YC,YD | 100 | 150 | | |

Notes:

- The default output follower current for each output is 0.96 ma. If the outputs are twinned, the user can select 1.92 ma.
- The user should note that different R_{SF} , R_{ST} and K values apply for Hi-Drive Macros.

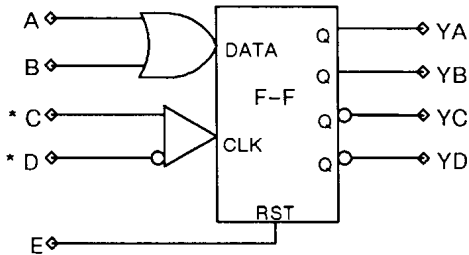
| INPUT | NUMBER OF AC LOADS | | Actual Capacitance |
|-------|--------------------|-----------|--------------------|
| | 1st LEVEL | 2nd LEVEL | |
| A | 1 | | 0.09 pF |
| B | 1 | | 0.09 pF |

TRUTH TABLE

| A | B | YA,YB | YC,YD |
|---|---|-------|-------|
| L | L | ND | ND |
| L | H | L | H |
| H | L | H | L |
| H | H | ND | ND |

NOTE: ND = NOT DEFINED

MACRO: 711 D FLIP-FLOP WITH GATED DATA INPUT AND DIFFERENTIAL CLOCK
1/2 CELL
2 LEVEL SERIES GATING



POWER: (mW)
H Macro 16.0

| MACRO DELAYS (ps) | | L MACRO | | H MACRO | |
|-----------------------|-------|---------|-----|---------|-----|
| IN | OUT | (+) | (-) | (+) | (-) |
| C,D | YA,YB | | | 300 | 350 |
| C,D | YC,YD | | | 300 | 325 |
| E | YA,YB | | | -- | 575 |
| E | YC,YD | | | 575 | |
| MIN CLOCK PULSE WIDTH | | | | 300 | |
| MIN RESET PULSE WIDTH | | | | 550 | |
| DATA SET UP | | | | 200 | |
| DATA HOLD | | | | 100 | |
| MIN RESET HOLD | | | | 100 | |
| MIN RESET RECOVERY | | | | 200 | |

Notes:

- The default output follower current for each output is 0.48 ma. If the outputs are twinned, the user can select 0.96 ma.
- Minimum reset hold time is the minimum amount of time that RESET must be held 'high' after the CLOCK switches from a 'low' to a 'high' in order for the flip-flop to remain in the reset state.
- It should be noted that the Master portion of the flip-flop is asynchronously reset when the RESET line is 'high'. This reset scheme eliminates the possibility of an output glitch for the condition: RESET = 'H', DATA = 'H', and the CLOCK transitions from 'L' → 'H'.

| INPUT | NUMBER OF AC LOADS | | Actual Capacitance |
|-------|--------------------|-----------|--------------------|
| | 1st LEVEL | 2nd LEVEL | |
| A | 1 | | 0.09 pF |
| B | 1 | | 0.09 pF |
| C | | 1 | 0.07 pF |
| D | | 1 | 0.07 pF |
| E | 1 | | 0.09 pF |

TRUTH TABLE

| RESET | DATA | CLOCK | | Q |
|-------|------|-------|-----|----|
| E | A+B | C | D | YA |
| L | X | H | L | -- |
| L | X | L | H | -- |
| L | L | L→H | H→L | L |
| L | H | L→H | H→L | H |
| H | X | H | L | L |
| H | X | L | H | -- |
| H | H | L→H | H→L | L |

NOTE: -- = NO CHANGE

MCA3 ETL MACRO LIBRARY LISTING

SIZE indicates the macrocell size in universal (U) cells for I/O macros and in quarter cells for the internal major (M) macrocells.

SG indicates the levels of series gating used in the macrocell function. Note that a '3' in this column denotes a macro which uses three-level series gating and thus cannot be used with a supply voltage of -4.5 Vdc. All three-level series gated functions are indicated by shading.

TABLE 6 - ECL/PECL I/O MACROS

| Macro | Function | Size | SG |
|--|---|-----------|----|
| INPUT INTERFACE (C) MACROS | | | |
| L/HC01 | INPUT BUFFER (Non-Inverting) Quad Buffer | 1-U CELL | 1 |
| L/HC02 | INPUT BUFFER (Inverting) Quad Buffer | 1-U CELL | 1 |
| L/HC03 | INPUT BUFFER (Inverting, Non-Inverting) | 1-U CELL | 1 |
| L/HC05 | DUAL DIFFERENTIAL INPUT BUFFER | 2-U CELLS | 1 |
| L/HC13 | DIFFERENTIAL INPUT BUFFER | 2-U CELLS | 1 |
| LC15 | DIFFERENTIAL BYPASS | 2-U CELLS | 1 |
| L/HC50 | INPUT LATCH with ENABLE LOW | 1-U CELL | 1 |
| LC70 | DIFFERENTIAL INPUT BUFFER WITH OFF CHIP TERMINATION INPUTS (High Drive) | 2-U CELLS | 1 |
| OUTPUT DRIVERS (E) MACROS, 60 & 50 ohm | | | |
| L/HE01 | 2-INPUT OR | 1-U CELL | 1 |
| L/HE02 | 2-INPUT NOR | 1-U CELL | 1 |
| L/HE03 | 4-INPUT OR | 1-U CELL | 1 |
| L/HE04 | 4-INPUT NOR | 1-U CELL | 1 |
| L/HE05 | 2 to 1 MUX | 1-U CELL | 2 |
| L/HE06 | 2-2 OR/AND | 1-U CELL | 2 |
| L/HE07 | 2-2 OR/EXOR | 1-U CELL | 2 |
| HE08 | 2 to 1 MUX with ENABE LOW (Inverting)) | 1-U CELL | 2 |
| HE09 | 2 to 1 MUX with ENABLE LOW (Non-Inverting) | 1-U CELL | 2 |
| L/HE10 | 2-2 OR/NAND | 1-U CELL | 2 |
| L/HE11 | 2 to 1 MUX with ENABLE LOW | 1-U CELL | 2 |
| L/HE12 | DIFFERENTIAL OUTPUT BUFFER | 2-U CELL | 1 |
| L/HE50 | D LATCH with CLOCK ENABLE LOW | 1-U CELL | 2 |
| HE70 | DIFFERENTIAL OUTPUT BUFFER | 2-U CELLS | 1 |
| HE71 | OPEN COLLECTOR DIFFERENTIAL OUTPUT BUFFER | 2-U CELLS | 1 |
| LE75 | OFF-CHIP TERMINATION PAD | 1-U CELL | 1 |
| CUTOFF OUTPUT (ZE) MACROS, 50 & 25 ohm | | | |
| ZE00 | 4-INPUT OR (50 ohm) | 1-U CELL | 1 |
| ZE50 | 4-INPUT OR (25 ohm) | 1-U CELL | 2 |
| STEEL I/O (S) MACROS | | | |
| LS00 | 2-INPUT OR | 1-U CELL | 1 |
| LS50 | INPUT BUFFER | 1-U CELL | 1 |
| BIDIRECTIONAL I/O (B) MACROS, 50 & 25 ohm | | | |
| HB26 | 2-2 OR/AND with INPUT BUFFER (50 ohm output) | 1-U CELL | 2 |
| HB27 | 2-2 OR/NAND with INPUT BUFFER (50 ohm output) | 1-U CELL | 2 |
| HB28 | 2 to 1 MUX LOW ENABLE with INPUT BUFFER (50 ohm output) | 1-U CELL | 2 |
| HB29 | 4-INPUT OR with INPUT BUFFER (50 ohm output) | 1-U CELL | 1 |
| HB30 | 4-INPUT NOR with INPUT BUFFER (50 ohm output) | 1-U CELL | 1 |
| HB50 | 4-INPUT OR with INPUT BUFFER (25 ohm cutoff output) | 1-U CELL | 2 |
| HB51 | 4-INPUT NOR with INPUT BUFFER (25 ohm cutoff output) | 1-U CELL | 2 |
| HB76 | 4-INPUT OR with INPUT BUFFER (50 ohm cutoff output) | 1-U CELL | 1 |

TABLE 7 — TTL & PECL I/O MACROS

| Macro | Function | Size | SG |
|---|---|----------|----|
| INPUT TTL TO ECL (T: 00–29) MACROS | | | |
| L/HT00 | TRANSLATOR with True and Complement | 1-U CELL | 1 |
| OUTPUT ECL TO TTL (T: 30–59) MACROS | | | |
| L/HT30 | NOR TRANSLATOR | 1-U CELL | 1 |
| L/HT31 | NOR TRANSLATOR with TTL Tri-State Enable | 1-U CELL | 1 |
| L/HT33 | OR TRANSLATOR | 1-U CELL | 1 |
| L/HT36 | OR TRANSLATOR with ECL Tri-State Enable | 1-U CELL | 2 |
| L/HT37 | NOR TRANSLATOR with ECL Tri-State Enable | 1-U CELL | 2 |
| BIDIRECTIONAL I/O (T: 60–89) MACROS | | | |
| L/HT60 | ECL 2-INPUT NOR TRANSLATOR and TTL to ECL INPUT BUFFER with TTL Tri-State Enable | 1-U CELL | 1 |
| L/HT63 | ECL 2-INPUT OR TRANSLATOR and TTL to ECL INPUT BUFFER with ECL Tri-State Enable | 1-U CELL | 1 |
| L/HT64 | ECL 2-INPUT NOR TRANSLATOR and TTL to ECL INPUT BUFFER with ECL Tri-State Enable | 1-U CELL | 1 |
| ECL TO TRI-STATE CONTROL (T: 90) MACRO | | | |
| L/HT90 | ECL to Tri-State Control NOR TRANSLATOR | 1-U CELL | 1 |
| INPUT TTL TO PECL (P: 00–29) MACROS | | | |
| L/HP00 | TRANSLATOR with True and Complement | 1-U CELL | 1 |
| OUTPUT PECL TO TTL (P: 30–59) MACROS | | | |
| L/HP30 | NOR TRANSLATOR | 1-U CELL | 1 |
| L/HP33 | OR TRANSLATOR | 1-U CELL | 1 |
| L/HP36 | OR TRANSLATOR with PECL Tri-State Enable | 1-U CELL | 1 |
| L/HP37 | NOR TRANSLATOR with PECL Tri-State Enable | 1-U CELL | 1 |
| BIDIRECTIONAL I/O (P: 60–89) MACROS | | | |
| L/HP63 | PECL 2-INPUT OR TRANSLATOR and TTL to PECL INPUT BUFFER with PECL Tri-State Enable | 1-U CELL | 1 |
| L/HP64 | PECL 2-INPUT NOR TRANSLATOR and TTL to PECL INPUT BUFFER with PECL Tri-State Enable | 1-U CELL | 1 |

TABLE 8 — INTERNAL MACROS

| INTERNAL MACROS (M-Cells) | | | |
|----------------------------------|------------------------|-----------|----|
| Macro | Function | Size | SG |
| L/H200 | 5-INPUT OR/NOR | 1/4 CELL | 1 |
| L/H201 | 4-INPUT OR/NOR | 1/4 CELL | 1 |
| L/H202 | 2-INPUT OR/NOR | 1/4 CELL | 1 |
| L/H203 | 8-INPUT OR/NOR | 1/2 CELL | 2 |
| L204 | 12-INPUT OR/NOR | 1/2 CELL | 1 |
| L/H207 | 6-INPUT OR/NOR | 1/4 CELL | 2 |
| L/H211 | 2-2 OR/AND | 1/4 CELL | 2 |
| L/H212 | 3-2-2 OR/AND | 1/2 CELL | 2 |
| L213 | 4-3-3 OR/AND | 1/2 CELL | 1 |
| L/H214 | 2-2-2-2-1-1-1-1 OR/AND | FULL CELL | 2 |
| L/H215 | 2-2-3-3-3 OR/AND | FULL CELL | 2 |
| L/H216 | 4-2-3-2-3 OR/AND | FULL CELL | 2 |
| L217 | 5-4-3-2 OR/AND | 1/2 CELL | 1 |
| L/H218 | 5-4-3-2-1 OR/AND | FULL CELL | 2 |
| L/H219 | 3-3 OR/AND | 1/4 CELL | 2 |
| L/H221 | 2-2 OR/EXOR | 1/4 CELL | 2 |
| L/H222 | DUAL 2-2 OR/AND/EXNOR | FULL CELL | 2 |
| L/H223 | 4-INPUT EXNOR | 1/2 CELL | 2 |
| L/H224 | 4-INPUT EXOR | 1/2 CELL | 2 |
| L/H225 | 2-1-1-2 OR/AND/EXOR | 1/2 CELL | 2 |

TABLE 8 - INTERNAL MACROS [continued]

INTERNAL MACROS (M-Cells)

| Macro | Function | Size | SG |
|--------|---|-----------|----|
| L/H226 | 2-1-1-2 OR/AND/EXNOR | 1/2 CELL | 2 |
| L/H227 | 2-1 EXOR/AND/NAND | 1/2 CELL | 2 |
| L/H228 | 2-1 AND/EXOR | 1/4 CELL | 2 |
| L251 | 4-TO-1 MUX W/ENABLE (LOW) | 1/2 CELL | 2 |
| L/H252 | QUAD 2-TO-1 MUX | FULL CELL | 2 |
| L/H253 | 2-TO-1 MUX W/ENABLE (LOW) | 1/4 CELL | 2 |
| L/H254 | 2-TO-1 MUX W/GATED INPUTS | 1/4 CELL | 2 |
| L/H255 | DUAL 2-TO-1 MUX W/COM. SELECT | 1/2 CELL | 2 |
| L/H256 | 2-TO-1 MUX | 1/4 CELL | 2 |
| L258 | 4-TO-1 MUX W/ENABLE (HIGH) | 1/2 CELL | 2 |
| L/H259 | 4-TO-1 MUX | 1/2 CELL | 2 |
| L/H261 | 1-OF-4 DECODER W/ENABLE (LOW) | 1/2 CELL | 2 |
| L/H262 | 1-OF-4 DECODER W/ENABLE (HIGH) | 1/2 CELL | 2 |
| L/H263 | 1-OF-4 DECODER (HIGH) | FULL CELL | 2 |
| L/H277 | 4-2-4-2-4-2 OR/AND | 3/4 CELL | 2 |
| L/H278 | 3 DATA INPUT DATA LATCH | 1/4 CELL | 2 |
| L/H279 | 4-2-4-2-4-2-4-2 OR/AND | FULL CELL | 2 |
| L/H280 | 4-2-4-2 OR/AND | 1/2 CELL | 2 |
| L/H281 | FULL ADDER | FULL CELL | 2 |
| L/H282 | FULL ADDER W/GATED INPUTS | 1/2 CELL | 2 |
| L/H283 | 2-BIT LOOK-AHEAD CARRY | FULL CELL | 2 |
| L/H284 | HALF ADDER W/GATED INPUTS | 1/4 CELL | 2 |
| L/H285 | 3-BIT ADDER (SUM) | 1/2 CELL | 2 |
| L/H286 | 3-BIT ADDER (CARRY) | 1/2 CELL | 2 |
| L/H290 | D FLIP-FLOP WITH SET AND RESET | 1/2 CELL | 2 |
| L/H291 | D FLIP-FLOP WITH RESET | 1/2 CELL | 2 |
| L/H292 | D FLIP-FLOP WITH MUX | 3/4 CELL | 2 |
| L/H293 | D LATCH WITH RESET | 1/4 CELL | 2 |
| L/H294 | D LATCH WITH MUX | 1/2 CELL | 2 |
| L/H295 | GATED 2-WAY D LATCH | 1/2 CELL | 2 |
| L/H296 | EXNOR D LATCH | 1/2 CELL | 2 |
| L/H297 | GATED 4-WAY D LATCH | 3/4 CELL | 2 |
| L/H298 | DUAL D LATCH W/RESET | 1/2 CELL | 2 |
| L302 | INPUT OR/NOR (High Drive) | 1/2 CELL | 1 |
| L/H310 | 4-4-4-4 OR/AND | FULL CELL | 1 |
| L/H311 | 3-3-3-3 AND/OR | FULL CELL | 2 |
| L/H312 | 3-3-3 AND/OR | 1/2 CELL | 2 |
| L/H313 | 2-2 OR/AND | 1/4 CELL | 2 |
| L/H315 | 2-2-1-1 OR/AND | 1/2 CELL | 2 |
| L/H318 | 3-3 AND/OR | 1/2 CELL | 1 |
| L319 | 3-3-2-1 AND/OR | 1/2 CELL | 2 |
| L/H320 | 2-3-4-4 AND/OR W/ENABLE (HIGH) | FULL CELL | 2 |
| L/H321 | 6-6-4-4-2-2 OR/AND | FULL CELL | 2 |
| L322 | 3-3-3 AND/OR | 1/2 CELL | 1 |
| L/H323 | 3-2-2-2-2-3 AND/OR | FULL CELL | 2 |
| L/H324 | 5-5-5-5 AND/OR | FULL CELL | 1 |
| L328 | 2-1 AND/EXOR (High Drive) | 1/2 CELL | 2 |
| L/H331 | 3-2-2 AND/OR | 1/2 CELL | 2 |
| L/H332 | GATED OR | 1/2 CELL | 2 |
| L/H333 | GATED OR | 1/2 CELL | 2 |
| L/H370 | DIFFERENTIAL LINE RECEIVER | 1/4 CELL | 2 |
| L/H371 | 2-1 MUX WITH DIFFERENTIAL INPUTS | 1/4 CELL | 2 |
| L/H372 | D FLIP-FLOP W/DIFFERENTIAL CLOCK AND DATA | 1/2 CELL | 2 |
| L/H373 | 2-1 MUX W/DIFF INPUTS AND DIFF MUX CTL | 1/4 CELL | 2 |
| L/H374 | DIFFERENTIAL LINE RECEIVER | 1/4 CELL | 1 |
| L/H375 | D FLIP-FLOP WITH DIFFERENTIAL CLOCK | 1/2 CELL | 2 |
| L/H376 | D FLIP-FLOP WITH DIFFERENTIAL CLOCK | 1/2 CELL | 2 |
| L380 | NOR LATCH | 1/4 CELL | 1 |
| L/H381 | D FLIP-FLOP WITH SET | 1/2 CELL | 2 |
| L/H391 | D FLIP-FLOP, NEGATIVE EDGE TRIGGERED | 1/2 CELL | 2 |

TABLE 8 - INTERNAL MACROS [continued]

INTERNAL MACROS (M-Cells)

| Macro | Function | Size | SG |
|--------|--|-----------|----|
| L/H392 | D FLIP-FLOP WITH MUX, NEGATIVE EDGE TRIGGERED | 3/4 CELL | 2 |
| L/H393 | D LATCH WITH CLOCK ENABLE (HIGH) | 1/4 CELL | 2 |
| L/H394 | D FLIP-FLOP WITH MUX, NEGATIVE EDGE TRIGGERED | FULL CELL | 2 |
| L/H395 | D FLIP-FLOP WITH ASYN SET AND DATA ENABLE | FULL CELL | 2 |
| L/H396 | SCAN D FLIP FLOP | FULL CELL | 2 |
| L/H397 | D LATCH WITH ASYN SET | 1/4 CELL | 2 |
| L/H398 | SCAN D LATCH W/ASYN SET | 1/2 CELL | 2 |
| L/H400 | 12-INPUT OR | 1/4 CELL | 2 |
| L/H401 | 12-INPUT NOR | 1/4 CELL | 2 |
| L402 | 2-INPUT OR/NOR, 3-INPUT OR/NOR | 1/4 CELL | 1 |
| L/H403 | 8-INPUT OR/NOR | 1/4 CELL | 1 |
| L/H404 | 12-INPUT NOR | 1/2 CELL | 3 |
| L/H411 | 2-2-2 OR/AND | 1/4 CELL | 3 |
| L/H413 | 4-3-3-3 OR/AND | 1/2 CELL | 2 |
| L414 | 3-3-3-3 OR/AND | 1/2 CELL | 2 |
| L/H416 | 4-2-3-2-3 OR/AND | FULL CELL | 3 |
| L/H417 | 5-4-3-2 OR/AND | 1/2 CELL | 2 |
| L/H418 | 5-4-3-2-1 OR/AND | 3/4 CELL | 2 |
| L/H419 | 4-4 OR/AND | 1/4 CELL | 2 |
| L421 | DUAL EXOR | 1/4 CELL | 2 |
| L/H422 | DUAL 2-2 OR/AND/EXOR | 1/2 CELL | 3 |
| L/H424 | 6-INPUT EXNOR | 1/2 CELL | 3 |
| L/H425 | 6-INPUT EXOR | 1/2 CELL | 3 |
| L/H427 | 2-1 EXOR/AND/NAND | 1/4 CELL | 3 |
| L/H438 | 6-5-4-3-2-1 OR/AND | 1/2 CELL | 3 |
| L/H451 | 4-1 MUX W/ENABLE(LOW) | 1/2 CELL | 3 |
| L452 | QUAD 2-TO-1 MUX | 1/2 CELL | 2 |
| L/H453 | 2-TO-1 MUX W/ENABLE(LOW) | 1/4 CELL | 3 |
| L/H454 | 2-TO-1 MUX W/ENABLE(HIGH) | 1/4 CELL | 3 |
| L/H455 | DUAL 2-TO-1 MUX W/ENABLE (HIGH) | 1/2 CELL | 3 |
| L456 | TRIPLE 2-TO-1 MUX(COMMON SELECT) | 1/2 CELL | 2 |
| L457 | TRIPLE 2-TO-1 MUX | 1/2 CELL | 2 |
| L/H458 | 4-1 MUX W/ENABLE(HIGH) | 1/2 CELL | 3 |
| L/H459 | DUAL 4-1 MUX | 1/2 CELL | 3 |
| L/H461 | 1-OF-4 DECODER WITH ENABLE(LOW) | 1/2 CELL | 3 |
| L/H462 | 1-OF-4 DECODER WITH ENABLE(HIGH) | 1/2 CELL | 3 |
| L464 | 8-3 ENCODER | FULL CELL | 3 |
| L/H465 | 1-OF-4 DECODER WITH ENABLE(LOW) | 1/2 CELL | 3 |
| L/H466 | 1-OF-4 DECODER WITH ENABLE(HIGH) | 1/2 CELL | 3 |
| L470 | DUAL 2-TO-1 MUX(COMMON SELECT) | 1/4 CELL | 2 |
| L474 | DIFFERENTIAL LINE RECEIVER (High Drive) | 1/2 CELL | 2 |
| L482 | TRIPLE FULL ADDER | FULL CELL | 2 |
| L/H485 | 3-BIT ADDER | 1/2 CELL | 3 |
| L/H501 | 2-INPUT OR (Quad Buffer) | 1/4 CELL | 1 |
| L/H502 | 2-INPUT NOR (Quad Buffer) | 1/4 CELL | 1 |
| L503 | 5x2 INPUT OR | 1/2 CELL | 1 |
| L/H510 | 4-4-4-4 OR/AND | 1/2 CELL | 2 |
| L/H511 | 3-3-3-3 AND/OR | 1/2 CELL | 3 |
| L/H512 | 3-3-3 AND/OR | 1/2 CELL | 3 |
| L/H513 | 3-1-1-1 OR/AND | 1/4 CELL | 2 |
| L/H518 | 3-3 AND/OR | 1/4 CELL | 2 |
| L/H519 | 3-3-2-1 AND/OR | 1/2 CELL | 2 |
| L/H520 | 2-3-4-4 AND/OR W/ENABLE(HIGH) | 1/2 CELL | 3 |
| L/H523 | 3-2-2-2-3 AND/OR | FULL CELL | 3 |
| H553 | 2-TO-1 MUX W/ENABLE LOW | 1/4 CELL | 2 |
| L/H571 | 8-OUTPUT BUFFER W/DIF INPUT & ENABLE (Quad Buffer) | 1/2 CELL | 3 |
| L585 | D FLIP-FLOP W/2to 1 MUX DATA INPUT | 1/2 CELL | 2 |
| L593 | W BUFFER | 1/4 CELL | 1 |
| L/H611 | 3-3-3 OR/AND | 1/4 CELL | 3 |
| L/H616 | 4-2-3-3-2 OR/AND | 1/2 CELL | 3 |

TABLE 8 – INTERNAL MACROS [continued]

INTERNAL MACROS (M-Cells)

| Macro | Function | Size | SG |
|--------|---|-----------|----|
| L/H618 | 5-4-3-2-1 OR/AND | 1/2 CELL | 3 |
| L/H658 | 4-1 MUX | 1/2 CELL | 3 |
| L/H685 | FULL ADDER W/GATED INPUTS | 1/2 CELL | 3 |
| L/H691 | D FLIP-FLOP W/RESET | 1/2 CELL | 2 |
| L/H692 | D FLIP-FLOP WITH MUX | 3/4 CELL | 2 |
| L/H694 | D FLIP-FLOP W/RESET (NEGATIVE HOLD TIME) | 1/2 CELL | 2 |
| L700 | DIFFERENTIAL LINE RECEIVER (High Drive) | 1/2 CELL | 2 |
| L701 | 2-TO-1 MUX W/DIFF INPUTS AND MUX CONTROL (High Drive) | 1/2 CELL | 2 |
| H710 | D FLIP-FLOP WITH DIFFERENTIAL CLOCK AND DATA | 1/2 CELL | 2 |
| H711 | D FLIP-FLOP W/GATED DATA INPUT AND DIFF CLOCK | 1/2 CELL | 2 |
| H712 | D FLIP-FLOP W/EXNOR GATED DATA INPUT & DIFF CLOCK | FULL CELL | 3 |
| L713 | D FLIP-FLOP W/DIFF CLOCK AND DATA (High Drive) | FULL CELL | 2 |
| L714 | D FLIP-FLOP W/ GATED DATA & DIFF CLK (High Drive) | FULL CELL | 2 |
| L/H802 | 3-INPUT EXOR/EXNOR | 1/4 CELL | 3 |
| L/H803 | 3-INPUT EXOR/EXNOR | 1/4 CELL | 3 |
| L804 | DUAL 2-INPUT AND | 1/4 CELL | 2 |
| L805 | DUAL 2-INPUT NAND | 1/4 CELL | 2 |
| L806 | DUAL 2-INPUT AND/NAND | 1/4 CELL | 2 |
| L807 | DUAL 2-INPUT AND/NAND | 1/4 CELL | 2 |
| L/H809 | 8-1 MUX WITH ENABLE (HIGH) | FULL CELL | 3 |
| L/H810 | 8-1 MUX WITH ENABLE (HIGH) | FULL CELL | 3 |
| L811 | DUAL 4-INPUT OR | 1/4 CELL | 1 |
| L812 | DUAL 4-INPUT OR/NOR | 1/4 CELL | 1 |
| L813 | DUAL 4-INPUT OR/NOR | 1/4 CELL | 1 |
| L814 | DUAL 4-INPUT NOR | 1/4 CELL | 1 |
| L815 | DUAL 2-INPUT OR | 1/4 CELL | 1 |
| L816 | DUAL 2-INPUT OR/NOR | 1/4 CELL | 1 |
| L817 | DUAL 2-INPUT OR/NOR | 1/4 CELL | 1 |
| L818 | DUAL 2-INPUT NOR | 1/4 CELL | 1 |
| L/H819 | 3-2-1 OR/AND | 1/4 CELL | 3 |
| L820 | 2-INPUT OR, 2-INPUT AND | 1/4 CELL | 2 |
| L850 | EXPANDABLE 2-1 MUX(CODER) AND 2x2-1 MUX | 1/2 CELL | 2 |
| L851 | EXPANDABLE 2-1 MUX | 1/2 CELL | 2 |
| L852 | EXPANDABLE 2-1 MUX | 1/2 CELL | 2 |
| L853 | EXPANDABLE 2-1 MUX | 1/2 CELL | 2 |
| L860 | EXPANDABLE 4-1 MUX(CODER) WITH ENABLE | 1/2 CELL | 3 |
| L/H861 | EXPANDABLE 4-1 MUX | 1/2 CELL | 3 |
| L/H862 | EXPANDABLE 4-1 MUX | 1/2 CELL | 3 |
| L/H863 | EXPANDABLE 4-1 MUX | 1/2 CELL | 3 |
| L870 | EXPANDABLE 8-1 MUX(CODER) | 1/2 CELL | 3 |
| L/H871 | EXPANDABLE 8-1 MUX | 1/2 CELL | 3 |
| L/H872 | EXPANDABLE 8-1 MUX | 1/2 CELL | 3 |
| L/H873 | EXPANDABLE 8-1 MUX | 1/2 CELL | 3 |
| L881 | DUAL D (INVERTING) FLIP-FLOP | 1/2 CELL | 2 |
| L882 | DUAL D FLIP-FLOP | 1/2 CELL | 2 |
| L893 | 3xD LATCH WITH COMMON CLOCK | 1/2 CELL | 2 |
| L/H894 | D LATCH WITH MUX | 1/4 CELL | 3 |
| L895 | D FLIP-FLOP | 1/4 CELL | 2 |
| L896 | 3xD LATCH WITH COMMON CLOCK AND RESET | 1/2 CELL | 2 |

TABLE – 9 DC ELECTRICAL CHARACTERISTICS

MCA3 ETL arrays are available in the following options:

- 100K, 100E operating at -4.5 Vdc (ECL) with 5.0 Vdc (TTL)
- 100K, 100E operating at -5.2 Vdc (ECL) with 5.0 Vdc (TTL)
- PETL Operating at +5.0 Vdc (PECL and TTL)

The power supply voltage limits for the following tables are:

- VCC = VCCO = 0 volts
- VEEE = -4.2 to -4.8 volts *or*
- VEEE = -4.784 to -5.616 volts
- VCCT = 4.75 to 5.25 volts
- VEET = 0 volts

ECL CHARACTERISTICS

100K COMPATIBLE OPTIONS – ECL OUTPUTS

| Symbol | Characteristic | Specification Limits | | | Unit |
|------------------|---------------------------------|-------------------------------|-------|-------|------|
| | | T _J = 25 to 115 °C | | | |
| | | Min | Typ | Max | |
| VOH ¹ | Output HIGH Voltage | -1025 | -955 | -880 | mV |
| VOH ² | Output HIGH Voltage (low power) | -1045 | -975 | -880 | mV |
| VOH ³ | Output HIGH Voltage (cutoff) | -1050 | -910 | -735 | mV |
| VOL | Output LOW Voltage | -1810 | -1705 | -1620 | mV |
| VOL ³ | Output LOW Voltage (cutoff) | -2020 | -1985 | -1950 | mV |
| VIH | Input HIGH Voltage | -1165 | | -850 | mV |
| VIL | Input LOW Voltage | -2020 | | -1475 | mV |

1. Standard (HE and HB macro) 50 ohm outputs terminated with a 50 ohm resistor to -2.0 volts or low power (LE macro) outputs terminated with a 68 ohm resistor to -2.0 volts.
2. Low power outputs with a 60 ohm external load to -2.0 volts.
3. Cutoff outputs are not compensated for temperature.

100K COMPATIBLE OPTIONS – STECL OUTPUTS (6mA AND 10mA CURRENT SOURCE)

| Symbol | Characteristic | Specification Limits | | | Unit |
|--------|---------------------|-------------------------------|-------|-------|------|
| | | T _J = 25 to 115 °C | | | |
| | | Min | Typ | Max | |
| VOH | Output HIGH Voltage | -1025 | -945 | -850 | mV |
| VOL | Output LOW Voltage | -1900 | -1785 | -1620 | mV |
| VIH | Input HIGH Voltage | -1165 | | -850 | mV |
| VIL | Input LOW Voltage | -2020 | | -1475 | mV |

1. STECL output levels are specified with no external load.
2. This table specifies levels for all STECL outputs.

DC CURRENT LIMITS – 100K COMPATIBLE OPTIONS

| Symbol | Input Forcing Voltages | Specification Limits | | Unit |
|------------------------|------------------------|---|--|------|
| | | T _J = 25 to 115 °C | | |
| I _{INH} Max | V _{IH} Max | I _{pull-down} + (N _L)(I _{input}) | | mA |
| I _{pull-down} | where: | 0.067 for standard input (75K pull-down) | | mA |
| I _{pull-down} | | 12.5 for 10 mA current source input | | mA |
| I _{pull-down} | | 7.5 for 6 mA current source input | | mA |
| N _L | | Number of DC unit loads connected to input | | UL's |
| I _{input} | | 0.005 | | mA |
| I _{INL} Min | V _{IL} Min | 0.5 | | µA |
| I _{EEE} | -- | CAD LIMIT | | -- |

TABLE – 9 DC ELECTRICAL CHARACTERISTICS [continued]

DC CURRENT AND RESISTOR LIMITS – STECL OUTPUTS AND INPUT CS

| Symbol | Characteristic | Specification Limits | | | Unit |
|---------------------|-----------------------|---|-----|------|------|
| | | T _J = 25 °C to T _J = 115 °C | | | |
| | | MIN | TYP | MAX | |
| I _{out 10} | STECL and Input CS | 8.0 | 10 | 12.5 | mA |
| I _{out 6} | STECL and Input CS | 4.5 | 6 | 7.5 | mA |
| R _{out 27} | STECL Series Resistor | 20 | 27 | 42 | ohms |
| R _{out 40} | STECL Series Resistor | 30 | 40 | 56 | ohms |

1. I_{out 10} and I_{out 6} refer to a 10 mA or 6 mA, respectively, internal current source for a STECL output or an input current source.
2. R_{out 27} and R_{out 40} refer to a 27 ohm or 40 ohm, respectively, internal series resistor at the output of a STECL driver.

TTL AND PECL CHARACTERISTICS

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE – TTL

| Symbol | Characteristic | Specification Limits | | | Unit | Test Conditions | |
|------------------------------|------------------------------|-------------------------------|------|------|------|--|--|
| | | T _J = 25 to 115 °C | | | | | |
| | | Min | Typ | Max | | | |
| V _{OH} | Output HIGH Voltage | 2.7 | 3.4 | -- | V | I _{OH} = -3.0mA | V _{CCT} = Min |
| V _{OL} | Output LOW Voltage | -- | 0.35 | 0.50 | V | I _{OL} = 12/24mA | V _{CCT} = Min |
| V _{IH} | Input HIGH Voltage | 2.0 | -- | -- | V | threshold over V _{CCT} and temp. range | |
| V _{IL} | Input LOW Voltage | -- | -- | 0.80 | V | threshold over V _{CCT} and temp. range | |
| V _{IK} | Input Clamp Diode Voltage | | | -1.2 | V | V _{CCT} = Min, I _{IN} = -18 mA | |
| I _{IH} ¹ | Input HIGH Current | -- | -- | 20 | µA | V _{CCT} = Max, V _{in} = 2.7 V | |
| I _{IL} ¹ | Input LOW Current | -- | -- | -400 | µA | V _{CCT} = Max, V _{in} = 0.5 V | |
| I _{OZH} | Output Off Current HIGH | -- | -- | 50 | µA | V _{CCT} = Max, V _{in} = 2.7 V | |
| I _{OZL} | Output Off Current LOW | -- | -- | -50 | µA | V _{CCT} = Max, V _{in} = 0.5 V | |
| I _{OS} ² | Output Short Circuit Current | -25 | -- | -150 | mA | 12 mA Driver | V _{CCT} = Max V _{out} = 0 |

1. Current per input.
2. Output should not be shorted for more than one second and no more than one output should be shorted at a time.

The power supply voltage limits for the following tables are:

$$V_{EE} = 0 \text{ volts} \qquad V_{CCE} = V_{CCO} = 4.75 \text{ to } 5.25 \text{ volts}$$

$$V_{CCT} = 4.75 \text{ to } 5.25 \text{ volts} \qquad V_{EET} = 0 \text{ volts}$$

PECL OUTPUTS

| Symbol | Characteristic | Specification Limits | | | Unit |
|------------------------------|---------------------------------|-------------------------------|-------------------------|-------------------------|------|
| | | T _J = 25 to 115 °C | | | |
| | | Min | Typ | Max | |
| V _{OH} ¹ | Output HIGH Voltage | V _{CCE} - 1025 | V _{CCE} - 955 | V _{CCE} - 880 | mV |
| V _{OH} ² | Output HIGH Voltage (low power) | V _{CCE} - 1045 | V _{CCE} - 975 | V _{CCE} - 880 | mV |
| V _{OH} ³ | Output HIGH Voltage (cutoff) | V _{CCE} - 1050 | V _{CCE} - 910 | V _{CCE} - 735 | mV |
| V _{OL} | Output LOW Voltage | V _{CCE} - 1810 | V _{CCE} - 1705 | V _{CCE} - 1620 | mV |
| V _{OL} ³ | Output LOW Voltage (cutoff) | V _{CCE} - 2020 | V _{CCE} - 1985 | V _{CCE} - 1950 | mV |
| V _{IH} | Input HIGH Voltage | V _{CCE} - 1165 | | V _{CCE} - 850 | mV |
| V _{IL} | Input LOW Voltage | V _{CCE} - 2020 | | V _{CCE} - 1475 | mV |

1. Standard (HE and HB macro) 50 ohm outputs terminated with a 50 ohm resistor to [V_{CCE} -2.0] volts, or low power (LE macro) outputs terminated with a 68 ohm resistor to [V_{CCE} -2.0] volts.
2. Low power outputs with a 60 ohm external load to [V_{CCE} -2.0] volts.
3. Cutoff outputs are not compensated for temperature.

TABLE 9 – DC ELECTRICAL CHARACTERISTICS [continued]

RECOMMENDED OPERATING CONDITIONS

| Symbol | Characteristic | Value | Unit |
|--------------------------------|--|------------|------|
| V _{EEE} | Supply Voltages (V _{CCE} = V _{CCO} = 0) for -4.5 V Options | -4.5 ± 0.3 | Vdc |
| V _{EEE} | Supply Voltages (V _{CCE} = V _{CCO} = 0) for -5.2 V Options | -5.2 ± 8% | Vdc |
| V _{CCE} | Supply Voltages (V _{EEE} = 0) for 5.0 V Options | 5.0 ± 5% | Vdc |
| V _{CCT} | TTL Supply Voltages for all Options | 5.0 ± 5% | Vdc |
| T _J | Operating Temperature (Functional) | 10 to 130 | °C |
| T _J | Junction Temperature (AC and DC Specs) | 25 to 115 | °C |
| t _r ,t _f | Max Clock Input Rise/Fall Times (20 to 80%) ECL | 5 | ns |
| t _r ,t _f | Max Clock Input Rise/Fall Times (10 to 90%) TTL | 15 | ns |

LIMITS BEYOND WHICH DEVICE LIFE MAY BE IMPAIRED

| Symbol | Characteristic | Value | Unit |
|------------------|--|-----------------------------|------|
| V _{EEE} | ECL Supply Voltage (V _{CCE} =V _{CCO} =0) | -7.0 to +0.5 | Vdc |
| V _{in} | ECL Input Voltage (V _{CCE} =V _{CCO} =0) | +0.5 to V _{EEE} | Vdc |
| V _{in} | ECL Input Voltage on Bidirectional (Cutoff) (V _{CCE} =V _{CCO} =0) ¹ | +0.5 to -2.0 | Vdc |
| V _{CCE} | PECL Supply Voltage (V _{EEE} =0) | -0.5 to +7.0 | Vdc |
| V _{in} | PECL Input Voltage (V _{EEE} =0) | V _{EEE} to +5.5 | Vdc |
| V _{in} | PECL Input Voltage on Bidirectional (Cutoff) (V _{EEE} =0) ¹ | +3.0 to +5.5 | Vdc |
| V _{CCT} | TTL Supply Voltage (V _{EET} =0) | -0.5 to +7.0 | Vdc |
| V _{in} | TTL Input Voltage (V _{EEE} =0) | -0.5 to +7.0 | Vdc |
| V _{out} | TTL Output Voltage | -0.5 to +5.5 | Vdc |
| I _{out} | ECL/PECL Output Source Current Continuous (50/60 ohm) | 30 | mA |
| I _{out} | ECL/PECL Output Source Current Surge (50/60 ohm) ² | 100 | mA |
| I _{out} | ECL/PECL Output Source Current Continuous (25 ohm) | 60 | mA |
| I _{out} | ECL/PECL Output Source Current Surge (25 ohm) ² | 200 | mA |
| I _{out} | ECL/PECL Output Source Current Continuous (STECL, 10 mA) | 5 | mA |
| I _{out} | ECL/PECL Output Source Current Surge (STECL, 10 mA) | 40 | mA |
| I _{out} | ECL/PECL Output Source Current Continuous (STECL, 6 mA) | 9 | mA |
| I _{out} | ECL/PECL Output Source Current Surge (STECL, 6 mA) | 44 | mA |
| I _{IN} | TTL Input Current | -30 to +5.0 | mA |
| I _{OL} | TTL Output Current | Twice Rated I _{OL} | mA |
| T _{stg} | Storage Temperature | -55 to +150 | °C |
| T _J | Junction Temperature (no time limit) | 165 | °C |
| T _J | Junction Temperature (<240 hours) | 250 | °C |

1. If a cutoff output is in the low (disabled) state and is being forced by an external driver, the forcing voltage must fall between V_{CCE} and -2.0 volts for ECL and V_{CCE} and +3.0V for PECL operation.

2. Surge current is defined as an output current between 30 mA and 100 mA for a 50/60 ohm output, 60 mA and 200 mA for a 25 ohm output, 5mA and 40 mA for a STECL (10mA), and 9 mA and 44 mA for a STECL (6mA). The surge current must last for less than 10µs and must have a duty cycle equal to or less than 1%.